Personal Information

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Summary

More than twenty five years of professional experience; industry and research institutions in Poland, Canada, Switzerland and Germany; signal processing; algorithm development; solutions for vision, radar and body & security; automotive industry; strong programming skills; ASIC design in full-custom style; artificial intelligence solutions; control systems, etc.

Education

2016 **Habilitation** in Electronics: "Analog and Analog-to-Digital Reconfigurable Low power Integrated Circuits Working in Parallel and/or in the Asynchronous Fashion", Technical University of Łódź, Poland [details]

2004 **PhD** in Telecommunications and Signal Processing (with distinctions): "Design and optimization of finite impulse response electronic filters integrated in the CMOS technology", Poznań University of Technology, Poland [details]

1991–1995 **M.Sc** in Control and Robotics: "Implementation of New Adaptive Algorithms for Control of Industrial Robots", Poznań University of Technology, Poland

Professional Experience

07/2014 – Present **Algorithm development / R&D / team leader**, *Aptiv Services Poland (former Delphi), Technical Center Kraków, Poland*

Automotive industry, Active Safety, Advanced Driver Assistance Systems, vision and radar data processing algorithms, body & security algorithms for door control zone, ITS, V2I, signal processing, AI-based solutions:

- Vision systems: algorithms for camera calibration, line detection including Bott's Dots, traffic sign recognition (TSR), speed estimation based on image processing, adaptive headlight control, etc.
- Radar solutions: barrier and obstacle tracking, determination of free zones for autonomous vehicles, new approaches to multi-domain data fusion, etc.
- Body & security solutions for door control zone: sensor-less rotation counting signal processing-based algorithm in brush commutated motors.
- Solutions for intelligent transportation systems / vehicle-to-infrastructure communication: algorithms for localization enhancement of road side units and vehicles on the road, solutions for autonomous mobility on demand and intelligent TSR system (optimizing network traffic).
- Solutions based on advanced techniques in mathematics and digital signal processing: linear and non-linear filters and filter banks, adaptive filters, Hough transform, wavelet transform, etc.
- A strong effort put on solutions optimized in terms of runtime for real time data processing and algorithms, including those suitable for low level hardware implementation.
- Investigations in the area of requirements for passive safety, in-car, equipment in the context of European New Car Assessment Program tests.
- Preparation and then realization of Polish government grant application (budget $>$ 9 million \$) for development of solutions suitable for autonomous driving and in active safety area.
- 23 patents published; 7 trade secrets; other publications (research, defensive); laureate of Innovation Hall of Fame (Aptiv) for outstanding patent achievements; [List of patents - Espacenet]
- C/C++, Matlab/Octave, Python, Polarion, JIRA

10/2010 – present **University Professor**, *Bydgoszcz University of Science and Technology, Faculty of Telecommunications and Electrical Engineering, Bydgoszcz, Poland*

R&D projects, teaching and student supervising (Bachelor, Master and PhD degrees).
Selected projects:

- ASIC development: circuits for artificial neural networks and signal processing, parallel and asynchronous solutions:
  - programmable, parallel, asynchronous circuit for determining topological distances in self-organizing neural networks and for the application in particle swarm optimization (PSO) algorithm,
  - programmable, parallel and asynchronous neighborhood function block,
  - adaptation mechanism of neuron weights,
  - programmable I/O block for described ASICs enabling multiplexing input and output pins.
- Software system for generating complex testing signals for verification of prototype programmable ASICs.
- Solutions for air pollution monitoring based on signal processing and artificial neural networks, suitable for low power hardware implementation.
- Solutions for advanced medical systems.
- C/C++, Matlab/Octave, Cadence, HSpice, LaTeX

10/1999 – 03/2000; 12/2012 – 02/2013; 07–08/2016 **R&D engineer**, *Industry institute IHP – Innovations for High Performance Microelectronics (formerly Institute für Halbleiterphysik) Frankfurt/Oder, Germany*

- Low power, low chip area, current mode, programmable 10-bit successive approximation (SAR) ADC and DAC implemented in CMOS technology.
- Low power, programmable multi-phase clock generator for the realized prototype SAR ADC.
- 1999 / 2000: Realization of a high data rate decimation FIR filter for ADC based on Σ-Δ modulator for the application in GSM base station (Matlab / Simulink, VHDL and transistor level implementation).

10/2002 – 06/2014 **Senior lecturer**, *College of Computer Science, Bydgoszcz, Poland*

- University courses taught: Programming languages (C/C++, Java for desktop systems and portable devices), Algorithms and data structures, Electronics, Multimedia systems, etc.
- Supervising students (Bachelor and Master degrees)

09/2008 – 08/2010; 01-03/2012 **Senior scientist, R&D design engineer, Invited Professor**, *University of Neuchâtel and Swiss Federal Institute of Technology in Lausanne (EPFL), Institute of Microtechnology (IMT), Electronics and Signal Processing Laboratory (ESPLAB), Switzerland*

Realized projects:

- Flywheel gyroscope: Levitated rotating MEMS for high sensitivity multi-axis gyroscope and multi-functional accelerometer (design and simulations of closed control loop of the gyroscope):
  - Analog-to-Digital Converter (ADC) based on $\Sigma - \Delta$ modulator working at 200 MHz,
  - multistage, multi-rate decimation filter of the ADC, designed also at the transistor level,
  - PID controller,
  - signal conditioning circuit - pulse width modulation approach,
  - out-of-loop, high order finite impulse response (FIR) filter for data extraction.
- Digital, fully parallel self-organizing neural network for the application in a new generation wireless body area network (WBAN) used in medical diagnostics.

09/2005 – 08/2008 **Postdoctoral fellow, research engineer**, *University of Alberta, Department of Electrical and Computer Engineering (ECE), Edmonton, Canada*

Realized projects:

- Analog front-end (AFE) VLSI ASIC for X-ray medical imaging applications in CMOS technology (pulse shaping filter, peak detector, asynchronous multiplexer with collision preventing mechanism)
- Ultra-low power Successive Approximation (SAR) Analog-to-Digital Converter (ADC) for the application to wireless sensor networks (WSN) and WBAN, as well as in the AFE chip used in medical imaging
- Analog and digital neural networks for the application in WBAN (CMOS technology, parallel and asynchronous solutions)
- Analog and digital filters for telecommunication and multimedia applications (switched-current and switched-capacitor solutions, 1-D and 2-D filters)

05/2006 – 06/2006 **Design engineer / internship**, *Scanimetrics, Edmonton, Canada*
Realization and optimization of a 2 GHz wireless transceiver and receiver in the CMOS 0.13 μm technology.

10/1996 – 09/2010 **Assistant Professor**, *Poznań University of Technology, Faculty of Telecommunications and Electrical Engineering, since 10/2001: Faculty of Control and System Engineering, Poznań, Poland*
R&D projects, teaching and student supervising.
Selected projects:

- Four ASICs realized in CMOS technology for the application in wireless communication (GSM receivers and base-station): analog and digital filters and filter banks (switched capacitor and switched current), multi-phase programmable clock generators, ADC based on Σ-Δ modulators.
- 2002 – 2004: "REsearch And Training Action for System On Chip DesigN (REASON)", 5^{th} Framework Program, European Union
- 2001 – 2003: "Optimization of Algorithms for Digital Speech Processing and its Enhancement for modern Telecommunication Systems and in Hearing Aids" – Polish government grant
- 1999 – 2001: "Design and Hardware CMOS and BiCMOS Realization of Analog Functional Blocks for GSM Receiver" – Polish government grant
- 1997 – 1999: European Union TEMPUS projects – scientific visits in ENIC Telecom, Lille-France and Centro Studi e Laboratori Telecomunicazioni (CSELT), Turin-Italy
- 1997: "New Methods for Separation and Filtering of Digital Signals Using Digital Signal Processors" – Polish government grant
- Cadence design framework, HSpice, VHDL (standard cell design for ASIC), Borland Pascal, C/C++

Honors, scholarships, awards

12/2012 – 02/2013 **DAAD (Deutscher Akademischer Austauschdienst) scholarship**, IHP Microelectronics, Frankfurt (Oder), Germany

2011 – 2012 **Foundation for Polish Science return grant**, UTP University of Science and technology, Bydgoszcz, Poland

09/2006 – 08/2009 **EU Marie-Curie International Outgoing Fellowship (IOF)**, Outgoing phase in Department of Electrical and Computer Engineering, University of Alberta in Edmonton, Canada. Return phase at the University of Neuchâtel and in EPFL, Switzerland. Contract with EPFL extended to 08/2010 after completing the scholarship

09/2005 – 08/2006 **Foundation for Polish Science fellowship**, Postdoctoral Fellowship granted yearly to 15 young Polish doctors. Department of Electrical and Computer Engineering, University of Alberta in Edmonton, Canada

2005 – 2008 **Grants for chip fabrication**, Four grants received from Canadian Microelectronics Corporation (CMC)

2002 and 2003 **Foundation for Polish Science scholarship**, Research scholarship granted by Foundation for Polish Science to 100 young Polish scientists for outstanding scientific achievements

2005 **Award**, Award of His Magnificence the Rector of the Poznań University of Technology for the best PhD thesis in 2004

2004 **Award**, PhD thesis with distinctions at the Poznań University of Technology

Skills & Background Knowledge

Technical skills

- C/C++ and Matlab/Octave programming languages used on a daily basis, Java used couple years ago,
- ASIC design tools – Cadence design system: Virtuoso layout editor, Schematics, Analog artist, Spectre simulator, Layout-versus-Schematics (LVS), SKILL programming language; Hspice transistor level simulator, etc.,
- Signal processing (1-D and 2-D signals) with practical industry and research applications,
- Long experience in advanced algorithm development,
- Real time data processing – automotive systems, solutions optimized for computational efficiency,
- VHDL used in the past and thus currently basic skills with ability to learn quickly,
- LaTeX high-quality typesetting system,
- More than 200 publications: journal and conference papers, book chapters, patents. [List of publications]

Personal skills

- High level in oral and formal written communication skills (English and Polish)
- Experience and abilities for team working
- Leading experience:
  - Delphi / Aptiv: Leading Vision Algorithm Development team, Advanced Engineering team, team of function owners, leader in investigations for ASICs for body security products, supervisor of industry PhD students.
  - Universities: Leading position in ASIC and algorithm development.

Interests / hobby

- Theology, Bible study and the ancient history of the Church
- Astronomy; Activity in the Mars Society Poland
- History (mainly XX century)
- Scouts instructor in Polish Scouting Association in Canada
- Tourism (hiking)
- Survival and bushcraft

I declare, that I agree to have my personal data, if it necessary, processed for recruitment process (according to the Act od personal data protection, dated 29 of August 1997, DzU nr 133, poz. 833).