

# Hardware Implementation of Selected Statistical Quantities for Applications in Automotive V2I Communication System

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*Abstract*— In this work we propose a concept of a transistor level implementation of a simplified iterative methods for computing several basic statistical quantities, such as the mean and the variance. The motivation behind the presented work is the realization of a calibration algorithm for determining the positions of the V2I (vehicle-to-infrastructure) communication devices in novel automotive applications. Such devices, mounted in fixed points of the road and urban infrastructure (RSU – road side equipment) will be used to support autonomous vehicles moving in urban and suburban environments. The role of the calibration procedure is to determine the positions of the RSU devices in global coordinate system (GCS) and save it in their internal memory blocks. To facilitate the hardware implementation, we introduced some modifications to existing (conventional) iterative algorithms used for the computation of the statistical quantities. For this purpose, we eliminated division operations, substituting them with bit shift operations. Shifting the bits may be easily realized fully asynchronously in hardware, using only a passive commutation field.

## I. INTRODUCTION

It is supposed that future active safety functions, which in recent years are intensively developed in the automotive industry, will be supported by the communication between vehicles and the road infrastructure (V2I – vehicle-to-infrastructure). In systems of this type one group of the communicating devices (RSU – road side units), mounted in the road infrastructure, will provide useful data to passing vehicles.

In the literature one can find many concepts of using the V2I system as a support for advanced driver assistance system (ADAS), and for the autonomous driving of vehicles in the future. In one of the simplest forms, it may rely on providing the vehicles relevant messages about dangerous situations on the road [2], [3]. They may include, for example, the risk of collision with a pedestrian or other vehicle, a traffic jam, an accident ahead, etc. In most advanced approaches, a framework

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of the RSU devices may actively participate in control of the trajectories of the autonomous vehicles. This option, however, requires a sufficiently dense network of the RSU devices playing the role of local navigation / orientation points. In this case, from a safety point of view, it is important to determine the position of these devices with respect to passing vehicles with relatively high precision. This problem is more and more frequently raised in the literature [4]–[7]. The vehicles have to distinguish whether they are recipients of the messages being transmitted over the network.

In our works, we focus on the development of the algorithms, that aim at increasing the efficiency and the quality of the positioning of the RSU devices in relation to passing vehicles. We rely on statistical methods based on repeated distance measurements to the stationary devices, carried out by passing vehicles. On the basis of a series of such measurements, it is also possible to initially calibrate the V2I system. A novel calibration algorithm of the V2I system has been recently reported by us in a patent application [1] (in progress in the European Patent Office). In contrary to state-of-the art solutions that propose the GPS as a support of such a system [4]–[6], we assume that the GPS is not necessarily required. This is due to some potential problems. One of them is often a reduced localization precision based on the GPS in dense urban area, in tunnels, etc., so that it is not always possible to rely on this system. Another question is how to effectively supply the RSU devices equipped with the GPS.

The last issue is related to the problem of energy consumption. We believe that circuits used in the RSU devices will have to be energy-efficient. This in practice means the need of a development of novel algorithms with low computational complexity. As a contribution, in one of our former works we have proposed simplified mathematical iterative methods for computing selected statistical quantities, such as the mean and the variance [8]. Based on a wide and comprehensive simulation investigations, we showed that with a sufficiently large number of the input samples, the errors introduced by the proposed methods do not exceed a few percent compared to the methods considered as classic [9].

The aim of this work is a novel hardware implementation of the described algorithms at the transistor level.

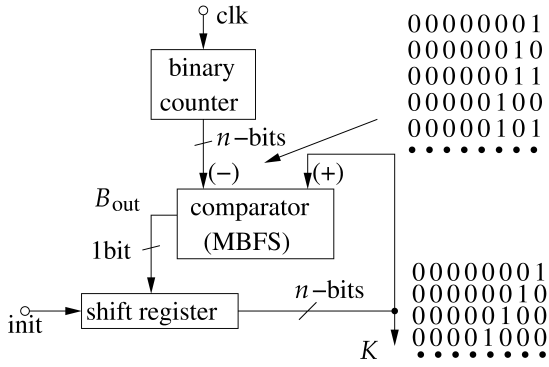


Fig. 1. A supporting circuit that controls denominator value in the mean and the variance circuits.

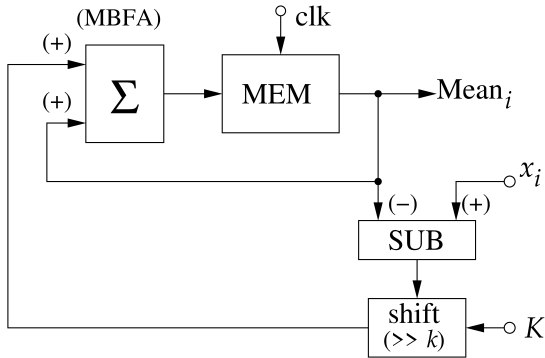


Fig. 2. The proposed, iterative circuit for the computation of the mean value.

In the comparison with conventional iterative methods, we use only simple arithmetical operations that include summing, subtracting and multiplying. The division operation has been eliminated and substituted with shifting the bits to the right by a number of positions that is automatically adapted to the number of the input samples.

## II. AN OVERVIEW OF THE PROPOSED METHODS FOR COMPUTING STATISTICAL QUANTITIES

Determining the location of the RSU devices can be performed through a direct communication between the RSU devices and the vehicles, based, for example, on such technologies as the impulse radio – ultra wide band (IR-UWB) one. This technology offers a relatively high positioning accuracy [10]. For this reason, it is considered as one of the technologies that may be used in the V2I communication [11], [12]. In this technique, the position of a device may be computed on the basis of the measurements of the time that elapsed between the transmission and the reception of the signal. When the measurements are repeated, and additionally the trajectory of the moving device (associated with the car)

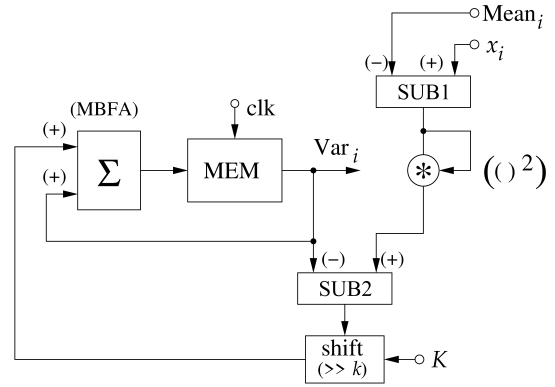


Fig. 3. The proposed, iterative circuit for the computation of the variance value.

is known, the use of the trilateration methods allow to compute the position of the RSU [11].

Theoretically, on the basis of a series of distance measurements the location of the RSU device can be unambiguously determined. In practice, various factors may affect the obtained results. The variation of external temperature and the noise may impact the response time of the devices, that will translate into a positioning error [13]. Due to these negative factors, a set of apparent positions of the RSU device is obtained. Based on them, the real location may be estimated by applying appropriate statistical computations.

In the proposed calibration algorithm [1] we assume that the statistical computations will be performed in particular RSU devices. Following,  $i^{\text{th}}$ , samples representing their apparent  $(x_i, y_i)$  positions in the global coordinate system (GCS) will be provided to these devices sequentially. In this situation iterative algorithms are the most appropriate. Due to expected hardware limitations we introduced some modifications to existing methods, as it is briefly presented below. The mean and the variance variables are initialized as follows:

$$\text{Mean}_1 = x_1 \quad (1)$$

$$\text{Var}_1 = 0 \quad (2)$$

where:  $x_1$  is a first recorded sample. The same computations are performed for the  $y$  coordinate in the GCS. For each new sample, the updates of these variables are computed in accordance with the following formulas:

$$\text{Mean}_i = \text{Mean}_{i-1} + [x_i - \text{Mean}_{i-1}]/i \quad (3)$$

$$\text{Var}_i = \text{Var}_{i-1} + [(x_i - \text{Mean}_{i-1})^2 - \text{Var}_{i-1}]/i \quad (4)$$

These equations, consistent with [9], require a division operation by the factor equal to the number of the

samples already processed. To eliminate the division operation in order to simplify the computation scheme, we replace the  $i$  factor with a new  $C$  variable [8]:

$$\text{Mean}_i = \text{Mean}_{i-1} + [x_i - \text{Mean}_{i-1}]/C \quad (5)$$

$$\text{Var}_i = \text{Var}_{i-1} + [(x_i - \text{Mean}_{i-1})^2 - \text{Var}_{i-1}]/C \quad (6)$$

which is initially set to 2 and then updated as follows:

$$\text{if } (i > C)\{C = C \cdot 2;\} \quad (7)$$

As a result, the  $C$  variable is always one of the powers of 2, i.e.  $C \in 2, 4, 8, 16, \dots$ . This variable allows for applying a much simpler operation, in which the terms in square brackets are shifted by  $k$  positions to the right ( $\gg$ ). This operation is the substitution of division by  $2^k$  factor. Finally we get:

$$\text{Mean}_i = \text{Mean}_{i-1} + [x_i - \text{Mean}_{i-1}] \gg k \quad (8)$$

and

$$\text{Var}_i = \text{Var}_{i-1} + [(x_i - \text{Mean}_{i-1})^2 - \text{Var}_{i-1}] \gg k \quad (9)$$

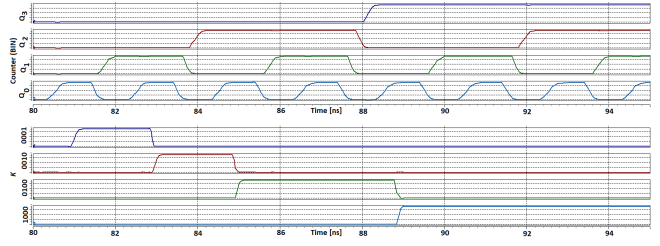
The  $k$  variable for each iteration is computed as follows ( $C = 2, k = 1$ , for  $i = 0$ ):

$$\text{if } (i > C)\{C = C \ll 1; k = k + 1;\} \quad (10)$$

### III. TRANSISTOR LEVEL IMPLEMENTATION OF THE PROPOSED ALGORITHMS

Formulas 8, 9 and 10 can be implemented relatively easily in the CMOS technology. Fig. 1 illustrates the circuit responsible for the adaptive change of the  $C$  and the  $k$  variables. It is based on a digital comparator, built on the basis of a multi-bit full subtractor (MBFS) and a 1-bit shift register. In Fig. 1 an additional variable  $K = C/2$  is introduced, as its particular bits directly control the ‘shift’ block.

When, as a result of the incrementing operation the output of the binary counter (provided to the negative input of the MBFS) becomes larger than the  $K$  variable, then the  $B_{\text{out}}$  (borrow out) bit becomes ‘1’. This signal shifts the bits in the  $K$  variable by one position and, consequently, modifies the  $C$  variable. For example, when  $K = 1$ , then the expressions in square brackets in 8 and 9 are shifted by one bit, which corresponds to the division by 2. After subsequent switches of the shift register, the variable  $K$  takes values: 2 (binary: Bx10), 4 (Bx100), 8 (Bx1000),  $\dots$ . This means that the expressions in [] in 8 and 9 are shifted by 2, 3, 4,  $\dots$  positions to the right, i.e. they are divided by 4, 8, 16,  $\dots$ , respectively. The ‘shift’ block was implemented as a commutation field composed of switches directly controlled by particular bits of the  $K$  signal.



| Counter (DEC) | Counter (BIN) | K (BIN) | C  |
|---------------|---------------|---------|----|
| 0             | 0000          | 0000    | 1  |
| 1             | 0001          | 0001    | 2  |
| 2             | 0010          | 0001    | 2  |
| 3             | 0011          | 0010    | 4  |
| 4             | 0100          | 0010    | 4  |
| 5             | 0101          | 0100    | 8  |
| 6             | 0110          | 0100    | 8  |
| 7             | 0111          | 0100    | 8  |
| 8             | 1000          | 0100    | 8  |
| 9             | 1001          | 1000    | 16 |
| 10            | 1010          | 1000    | 16 |
| 11            | 1011          | 1000    | 16 |
| 12            | 1100          | 1000    | 16 |
| 13            | 1101          | 1000    | 16 |
| 14            | 1110          | 1000    | 16 |
| 15            | 1111          | 1000    | 16 |

Fig. 4. Selected simulation results of the circuit shown in Fig. 1

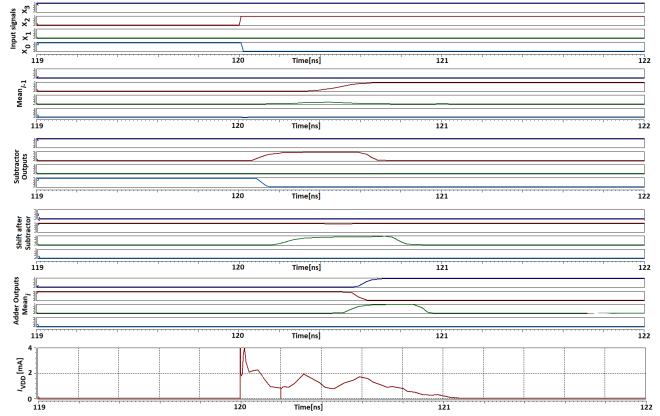


Fig. 5. Selected simulation results of the circuit shown in Fig. 2 illustrating computation time of a single cycle.

Fig. 4 presents selected transistor level simulation results of the circuit shown in Fig. 1, as well as a table with states of particular variables described above. This circuit throughout the  $K$  variable controls the circuits shown in Figs. 2 and 3 that are responsible for computing the mean and the variance, respectively. The circuit that computes the variance uses also the mean value calculated by the circuit shown in Fig. 2.

Both these circuits work on a similar principle. Since the algorithms are iterative, therefore an accumulator (ACU) has to be applied in the proposed circuits. In 8 and 9 the ACU is represented by the summing opera-

tion (before the square brackets). The ACU consists of a summing circuit, realized as an asynchronous multi-bit full adder (MBFA) and a memory block realized in this case on the basis of the D-flip flops. The memory is the only block in these circuits that are controlled by a 1-phase clock circuit. All other components operate fully asynchronously. This is illustrated in selected transistor-level simulations shown in Fig. 5 for the mean algorithm. As can be observed, the overall computation cycle between the input of the circuit and the output of the MBFA in the ACU takes about 1 ns. In case of the variance circuit this time is longer (2-3 ns) due to some additional blocks described below.

Of these two circuits, the variance one is more complex. The current value of the mean and a new signal sample  $x_i$  are provided to the inputs of this circuit. The circuit first calculates the difference between these signals in an asynchronous subtraction system (SUB1). The subtraction result is squared using a multiplier, which is realized as an asynchronous binary tree circuit. The multiplier operates in one-quadrant mode, that simplifies its structure. It is possible as the result of the squaring operation is independent of the sign of the difference between the sample  $x_i$  and the mean. If the subtraction result is negative, which is signaled by the borrow out bit of the MBFS signal used in the SUB1 block, the absolute value of this signal is calculated. It requires negation of all bits and adding '1', as this signal is coded with two's complement code.

At the next stage of the computation chain, the SUB2 block computes a difference between the square signal and the value of the variance computed in the previous iteration,  $\text{Var}_{i-1}$ . The output from SUB2 is coded in two's complement code, which means that negative numbers have the value '1' on the most significant bits (MSB). In this case, when shifting the bits to the right, the MSBs have to be supplemented with '1'. For a positive output of SUB2 block, the MSBs are supplemented with '0'. In practice, these bits are supplemented by the borrow out bit from the MBFS used in the SUB2 block. The final result of the described operations is added to the value stored in the ACU. In the following clock impulse the new value of the variance is stored in the memory of the ACU.

#### IV. CONCLUSIONS

In the paper we proposed a concept of a hardware implementation of iterative algorithms for calculating the mean and the variance statistical quantities. To facilitate this implementation, the classic algorithms have been modified so that to eliminate the division operation. This resulted in a relatively high data rates. The calculation time of a single sample of the mean and the variance does not exceed 4 ns, with an energy consumption at the level of about 4-10 pJ per single sample, depending on the resolution of the processed signals.

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