# Multi-Rate Signal Processing with the Use of Filter Banks Composed of Parallel FIR Filters

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*Abstract*— **The paper presents a concept of a hardware implementation of 2-D finite impulse response (FIR) filter banks for the application in image processing and analysis. Banks composed of low- and high-pass FIR filters are basic components of multi-stage discrete wavelet transform (DWT). The applications of such solutions that are in the scope of our interests are vision systems used in automotive active safety functions (e.g in line departure warning). Basics of the DWT are broadly described in the literature. In our work we focus on solutions supporting hardware realization of filter banks for DWT. The proposed parallel and asynchronous circuits allow to achieve the processing time for a single pixel not exceeding 2 to 4 ns, depending on the size of the mask (data for TSMC 180 nm CMOS process).**

## I. Introduction

Filtering of signals is one of basic operations performed in software and electronics systems. In fact, every digital system may be considered as a filter. Filters are used to process either continuous or discrete time signals, analog or digital (quantized and sampled in time). The properties of the processed signal, as well as the target application determine the type of the used filters, their mathematical parameters, as well as the way of their implementation. The last aspect, in this work understood as a hardware structure, strongly depends on such parameters of the frequency response as the cut-off frequency, the steepness in the transient band, the attenuation in the stopband, etc.

In this work we focus on the implementation of filter banks composed of FIR filters that may be used, for example, in discrete wavelet transform (DWT). Banks of this type are commonly applied in signal processing in many engineering areas [1]. In the scope of our interests are solutions for the intelligent transportation system (ITS). They include automotive active safety (AS) functions, autonomous driving and its interaction with the intelligent road and urban infrastructure. Pattern recognition that may be supported by the DWT is used, for example, in line departure warning (LDW), camera calibration and traffic sign recognition (TSR).

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In case of the application of filter banks in automotive area, it is necessary to pay attention to several important aspects. One of them is the need to process data in real time [2], so that the vehicle can quickly react to changing situation on the road. Another issue is the computational complexity, which should be kept as small as possible, taking into account the range of tasks typically performed by the vision system as well as hardware limitations that result from the final price of the system. In this context, the use of solutions based on application specific integrated circuits (ASIC) can play an important role – specialized co-processors speeding up selected signal processing tasks.

## II. Discrete wavelet transform and its applications – a brief overview

In the literature one can find examples of the application of the DWT in automotive and vision applications. One of them is a system that allows for an estimation of the occupancy of ad-hoc parking lots [3]. The system based on 2-D DWT is realized in field programmable gate array (FPGA) and exhibits low computation complexity. It demonstrates the ability of detecting objects when no background subtraction is applied. Another example is an in-vehicle monocular pre-crash vehicle detection system [4]. At one of the steps of this real-time procedure a simple Haar wavelet is used in the decomposition of the input signal for feature extraction and object classification. The reported system was successfully tested under different traffic scenarios, such as highway and urban environment and under varying weather conditions. The DWT can also be used in vehicle tracking systems in object detection on the basis of their motion [5], or more generally in optical flow applications [6]. In [5] the Gabor and the Mallat wavelets were used for improving the accuracy and speed of the vehicle detection. In [7] a robust vehicle detection system is proposed. In this case the fast wavelet transform (FWT) is used to extract image texture. Comparing the textures, different for the vehicles and the shadows allow to detect them.

The DWT is commonly realized as a cascade multi-rate operation, in which filter banks are applied alternately with downsampling operations, as illustrated in Fig. 1 for 1 dimensional (1-D) signal. In this example, the bank is composed of two complementary low-pass (LP) and high-pass (HP) FIR filters. Filters, filter

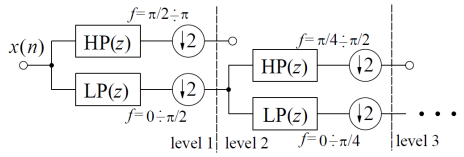


Fig. 1. Discrete wavelet transform realized as a multi-stage filtering with quadratic mirror filter (QMF) bank and downsampling operations.

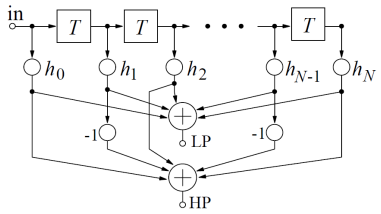


Fig. 2. Possibilities of the simplification of the QMF bank in case of symmetrical TFs.

banks and functions used in the vision systems are usually realized as functions in software systems, frequently in digital signal processors (DSP). In hardware one can find realizations in FPGAs [8], [3], [9] as well as in the full-custom style analog circuits [10].

One of important problems in hardware is the realization of the filter coefficients. Ratio between the largest and the smallest coefficient and the implementation precision directly impact the circuit complexity and the quality of the frequency response [11]. The precision here is related to a mapping of theoretical values of the coefficients into usually limited signal resolutions in a target hardware platform. In filters, that offer very large attenuation, the values at remote decimal places of the numbers representing the coefficients are important. In hardware, on the other hand, it is necessary to limit the precision, to avoid large circuit complexity. There exists a trade-off between these two factors.

In some vision applications, described above, simple Haar wavelets are used (an equivalent of the Daubechies (db1) wavelet), with 1 $^{st}$ order masks (length $L = 2$) with equal coefficients. However, in other applications more complex transfer functions (TF) may be required. An additional problem is that many wavelets feature unsymmetrical TF, which impose an additional challenge on the hardware realization. For a symmetrical TF of the FIR filter, the HP filter may be realized on the basis of the LP filter simply by the multiplication of each odd coefficient by -1 (see Fig. 2). It is not possible in unsymmetrical TF, in which the vector of the coefficients needs to be additionally mirrored. In our work we focus on symmetrical TFs, as we found that such filters are sufficient in our application.

In the case of image analysis in the DWT, in the decomposition phase, the input signal it is divided into four subbands. The input signal is first processed line by line with $(L \times 1)$ (L)ow pass and (H)igh pass filters. The two output signals, obtained in this way, are then filtered in columns also with 1-D filters of type L and H, forming four output signals that can be designated as LL, HL, LH and HH. In the case of the symmetrical TFs of the used filters, to calculate all subbands one can use a similar solution as shown in Fig. 2.

In this work we present a concept of a hardware realization of the QMF banks composed of FIR filters with symmetrical TFs. In our work we propose a parallel and additionally asynchronous solutions, that allow for a significant simplification of the controlling clock circuit, and at the same time ensure a high data rate.

## III. The proposed QMF bank

As mentioned earlier, in hardware realizations there exists a trade-off between the circuit complexity and the functionality at the system level. For this reason, in this work we consider 2-D filters with a flat frequency response, that allow for substantial simplification of the hardware structure, while in many situations offering good properties at the signal processing level. An example here is the use of simple Haar wavelets in some applications. The Haar wavelet is the simplest solution in which filters with symmetrical TFs may be used.

We assume that all input signal samples for a given computation cycle (under the filter mask) are available at the inputs of the filter bank. In the proposed solution, the outputs of all four filters (LL, HL, LH, HH) are then computed in four clock cycles only, as each of the filters operates asynchronously. A general structure of the proposed solution is shown in Fig. 3 (a). This circuit consists of 1-D FIR filters, whose structures for selected mask sizes are shown in diagrams (b) and (c). A set of the filter masks for the (3×3) is given as follows:

$$\begin{aligned} \mathrm{LL}_{(3\times3)} &= \begin{bmatrix} 1 & 2 & 1 \\ 2 & 4 & 2 \\ 1 & 2 & 1 \end{bmatrix} \quad \mathrm{LH}_{(3\times3)} = \begin{bmatrix} 1 & 2 & 1 \\ -2 & -4 & -2 \\ 1 & 2 & 1 \end{bmatrix} \\ \mathrm{HL}_{(3\times3)} &= \begin{bmatrix} 1 & -2 & 1 \\ 2 & -4 & 2 \\ 1 & -2 & 1 \end{bmatrix} \quad \mathrm{HH}_{(3\times3)} = \begin{bmatrix} 1 & -2 & 1 \\ -2 & 4 & -2 \\ 1 & -2 & 1 \end{bmatrix} \end{aligned} \tag{1}$$

Example filter masks for higher order filters with flat frequency response, for the $(4 \times 4)$, $(5 \times 5)$ and $(7 \times 7)$ cases respectively are as follows:

$$\mathrm{LL}_{(4\times4)} = \begin{bmatrix} 1 & 3 & 3 & 1 \\ 3 & 9 & 9 & 3 \\ 3 & 9 & 9 & 3 \\ 1 & 3 & 3 & 1 \end{bmatrix}, \mathrm{HH} = \begin{bmatrix} 1 & -3 & 3 & -1 \\ -3 & 9 & -9 & 3 \\ 3 & -9 & 9 & -3 \\ -1 & 3 & -3 & 1 \end{bmatrix} \tag{2}$$

$$\mathrm{HH}_{(5\times5)} = \begin{bmatrix} 1 & -4 & 6 & -4 & 1 \\ -4 & 16 & -24 & 16 & -4 \\ 6 & -24 & 36 & -24 & 6 \\ -4 & 16 & -24 & 16 & -4 \\ 1 & -4 & 6 & -4 & 1 \end{bmatrix} \tag{3}$$

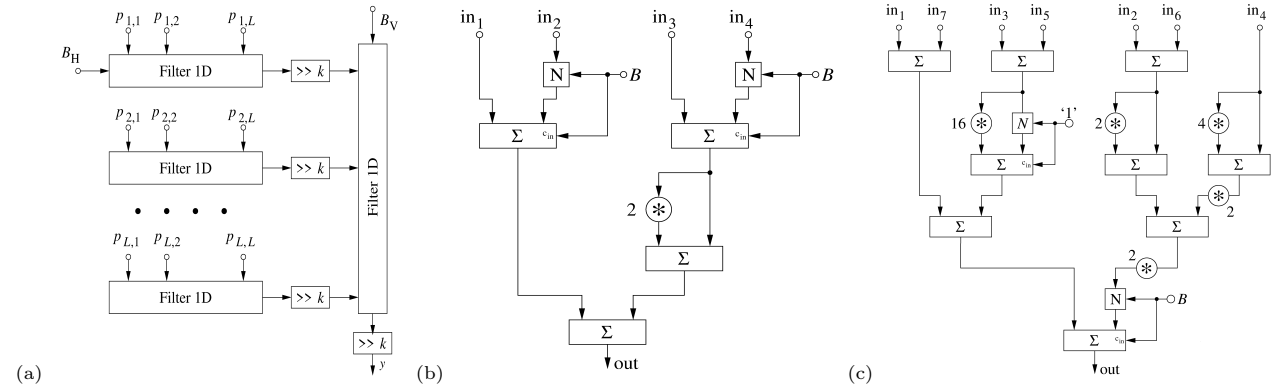


Fig. 3. The proposed solution for parallel and asynchronous filter bank: (a) a general block diagram of the 2-D filter bank, composed of a set of equal asynchronous 1-D FIR filters, (b) 1-D filter (mask: [1 (-)3 3 (-)1]) for the $(4 \times 4)$ case, (c) 1-D filter (mask: [1 (-)6 15 (-)20 15 (-)6 1]) for the $(7 \times 7)$ case.

Fig. 4. Results for proposed filter bank – LL, HL, LH and HH subbands, for L = [1 1] and H = [1 -1] 1-D filters. The results are presented for $2^{\text{nd}}$ stage of the DWT (decimation by 4 in each direction). (photo: own source).

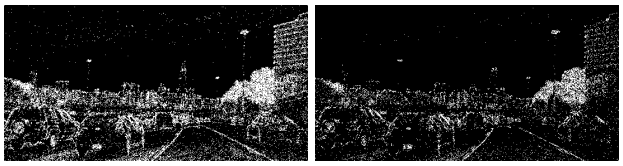

Fig. 5. Results for HH subband for (a) L = [1 2 1], H = [1 -2 1], (b) L = [1 3 3 1], H = [1 -3 -3 1].

$$\mathrm{LL}_{(7\times7)} = \begin{bmatrix} 1 & 6 & 15 & 20 & 15 & 6 & 1 \\ 6 & 36 & 90 & 120 & 90 & 36 & 6 \\ 15 & 90 & 225 & 300 & 225 & 90 & 15 \\ 20 & 120 & 300 & 400 & 300 & 120 & 20 \\ 15 & 90 & 225 & 300 & 225 & 90 & 15 \\ 6 & 36 & 90 & 120 & 90 & 36 & 6 \\ 1 & 6 & 15 & 20 & 15 & 6 & 1 \end{bmatrix} \quad (4)$$

One of main aspects presented in this work is how to realize these filters in a parallel and asynchronous way. It is shown in Fig. 3 for 1-D filters. The $L$ filters used in the rows in this circuit are equal to the one used in the column. The computation schemes for selected filters with flat frequency response are as follows:

$$\mathrm{out}_{(3\times1)} = (\mathrm{in}_1 + \mathrm{in}_2) + \beta \cdot (2 \cdot \mathrm{in}_3) \quad (5)$$

$$\mathrm{out}_{(4\times1)} = (\mathrm{in}_1 + \beta \cdot \mathrm{in}_4) + (1+2) \cdot (\mathrm{in}_3 + \beta \cdot \mathrm{in}_2) \quad (6)$$

$$\begin{aligned} \mathrm{out}_{(5\times1)} =& (\mathrm{in}_1 + \mathrm{in}_5) + ((1+2) \cdot \mathrm{in}_3) \cdot 2 + \\ & 4 \cdot (\mathrm{in}_2 + \mathrm{in}_2) \cdot \beta \end{aligned} \quad (7)$$

$$\begin{aligned} \mathrm{out}_{(7\times1)} =& (\mathrm{in}_1 + \mathrm{in}_7) + (\mathrm{in}_3 + \mathrm{in}_5) \cdot (16-1) + \\ & [(\mathrm{in}_2 + \mathrm{in}_6) \cdot (2+1) + \\ & \mathrm{in}_4 \cdot (4+1) \cdot 2] \cdot 2 \cdot \beta \end{aligned} \quad (8)$$

The input and the output signals are marked as in and out, respectively. The values of the input signal are expressed in two's complementary code. The summing operation is performed by the use of a multi-bit full adder operating in an asynchronous way. The filter coefficients have been expressed by means of sums of numbers that are powers of 2. It allowed us to realize the multiplication by appropriate bit shifting and summation. For example, multiplication by a factor of 6 is realized as the sum of a given input sample and the same sample after its shifting by one bit to the left, followed by another shift by 1 position to the left ($(1+2)\cdot2$). The multiplication by the 15 factor is realized as the difference of a given sample after the shift by 4 bits to the left (multiplication by 16) and this sample without the shift $(16-1)$. The presented computing diagrams have been designed in such a way, to minimize the number of the summation operations, which is important from the point of view of the circuit complexity.

An important here is to explain the meaning of the $\beta$ factor and the $B$ signals in Fig. 3. The $B$ signals may be either '0' or '1', depending on whether a given filter coefficient is positive or negative, respectively. Bits $B$ (index H and V for horizontal and vertical directions) are provided to some MBFAs as carry-in signals ($c_{\text{in}}$) in least significant 1-bit full adder. This operation, along with the negation of all bits of a given input pixel (in

block N), are the subtraction. To simplify the functional description of the presented circuits, we used the $\beta$ factor, which takes the values 1 or -1 for $B$ equal to 0 or 1, respectively.

The negation block (N) is implemented using NOT gates and switches. The multiplication operations realized as bit shifting do not require additional elements. The signal is simply provided to the inputs of a corresponding MBFA with an appropriate offset.

Circuit complexity for a given mask depends on the number of the used MBFAs. The (3×3) mask requires 2 summing operations in each 1-D filter (10 for the overall filter). For the masks $(4 \times 4)$, $(5 \times 5)$ and $(7 \times 7)$ these numbers are respectively, 20 (4 in 1-D direction), 30 (5 in 1-D) and 72 (9 in 1 -D). The output of each 1-D block is divided by the sum of the absolute values of all its coefficients, which in filters with flat frequency response always is a power of 2. Thus it may be carried out by shifting all bits of the output signal to the right by a given number of positions.

### A. Verification of the proposed solutions

The proposed systems have been verified by means of simulations at the signal processing level. For this purpose, the described calculation schemes have been reproduced with details in the simulator. Selected test results are shown in Figs. 4 and 5 for an example picture illustrating a road (authors' private source). The objective was to detect the boundaries of the current vehicle's line. A number of tests were carried out for the filter masks described above. The shown results are four subbands of the 2-D QMF bank at the second stage of the DWT. To better illustrate the HL, LH and HH components, the image was normalized. For the HH component, which is the most interesting here, binary thresholding has been applied. This facilitates a direct assessment and the comparison of performance of particular filters. Fig. 4 shows all subbands for the use of Haar wavelets i.e. the $(2 \times 2)$ mask, while Fig. 5 presents the HH component for the $(3 \times 3)$ and $(4 \times 4)$ filter masks. The observable trend is that filters with larger mask sizes (more selective) allow to achieve a higher signal-to-noise ratio – the boundaries of the line are more clearly visible on its background.

The circuit was tested in such a way that at the beginning the signals $B_{\mathrm{H}}$ and $B_{\mathrm{V}}$ were set to '0', thus the filter worked in the LL mode. After calculating the output signal, the $B$ signals were switched successively to states 01, 10 and 11, which allowed for the computation of remaining signal components for a given set of the input samples. In case of a transistor level implementation, for each combination of the $B$ signals, the filter further operates fully asynchronously. Thus, the data rate depends on the number of the maximum number of the summing circuits in a single path between the system inputs and its output. For a mask $(7 \times 7)$ for both 1-D filtering stages, the total number of MBFAs equals 8. In the CMOS 180 nm technology a single pixel is in this case computed in less than 4 ns. For smaller masks, this time is even half as long. For newer technologies, one can expect a significant improvement in these results. As in the DWT after each stage the signal is decimated, therefore the number of the output pixels that have to be computed for a single filter is amounted to only 1/4 of pixels of the input signal.

## IV. Conclusions

A concept of the 2-D filter bank for the application in image analysis in the automotive vision systems has been presented. An advantage of the proposed solutions is a parallel and asynchronous operation of the used filters that allows for achieving high data processing rates. A single filter mask can be easily switched between four filters used in the 2-D QMF bank in DWT.

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