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Programmable, switched-capacitor finite impulse response filter realized in CMOS technology for education purposes

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***Abstract*—The paper reports comprehensive laboratory tests of a mixed analog-digital, application specific integrated circuit (ASIC). The realized chip is a programmable device. It contains such components as an operational amplifier, a sample-and-hold (S&H) element, programmable array of capacitors, multiphase clock generator and a programmable switched capacitor (SC) delay line. All these blocks may be used separately or may be coupled together into a finite impulse response (FIR) filter, with reconfigurable frequency response. Since the filter coefficients may be either positive or negative, therefore both lowpass or highpass frequency responses may be obtained. The chip has been designed in the AMS CMOS 0.35 μm technology and occupies the area of 0.5 mm^2. It was designed for educational purposes. Programming and testing of the chip was made with the computer-controlled interface prepared in the National Instruments LabVIEW environment. The presented solutions allow for conducting of various laboratory exercises.**

***Index Terms*—Switched capacitor circuits, Programmable circuits, CMOS technology, Education**

I. INTRODUCTION

Analog discrete time filters in some cases can be an alternative to the similar digital solutions. In a typical real-signal processing scheme, the analog signal after a rough anti-aliasing filtering is converted to a digital form. Then it is subjected to more accurate processing, using fully digital blocks.

The use of more selective filtering at the analog side can, in certain situations, simplify the structure and requirements of an analog-to-digital converter (ADC), which is the next component in the signal processing chain. Discrete time filters of this type, such as finite impulse response (FIR) and infinite impulse response (IIR) filters, can be implemented in either the voltage or the current technique. In this work, we present a solution based on the first one – the switched capacitor (SC) technique [3].

Typical FIR and IIR filters are composed of a delay line or delay lines, blocks that multiply signal samples stored in the delay lines by filter coefficients, and a summing block. In the analog approach, all these operations have to be performed with analog signals. In the SC FIR filters, signal samples are stored as voltages on capacitors. Multiplication is carried out through appropriate ratios between capacities. The summation is realized using a capacitive summing system composed of an operational amplifier and capacitors.

The SC FIR filter designed and presented in this work is an example of such solutions. This project is a continuation of authors' previous works in this area. In previous approaches, however, we did not use programmable solutions. It resulted from the application of the realized projects in GSM base station, in which a proper attenuation in stop band of the frequency response was one of the key features [4]. While introducing programmable solutions, additional configuration switches have to be used to enable connecting or disconnecting of particular blocks. Such switches introduce inaccuracies, which are in particular visible in case of the analog circuits. For example, the capacitance of the capacitors used in the switches may affect the capacity of the coefficient capacitors (CCs), thus modifying the frequency response of the filter.

II. IMPLEMENTATION ISSUES OF FIR FILTERS

FIR filters are very commonly used in various areas of technology. The main element of these filters is the delay line, which stores consecutive samples of the input signal. Other elements are: the block of filter coefficients and the summing circuit. Signal samples from the delay line are multiplied by coefficients, which play role of weights. At the next stage, the results of the multiplication operations are summed and the result of this operation becomes the output of the filter.

Depending on the application, the implementation of these filters may be different. The most commonly filters of this type are realized in software. This is due to the a simplicity

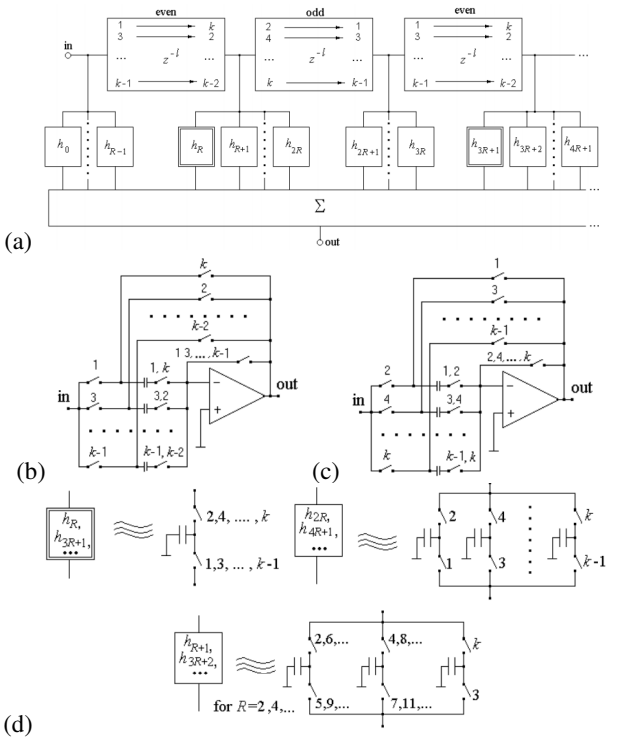

Fig. 1. Even-Odd SC FIR filter: (a) a general structure (b, c) even and odd delay elements, respectively, (d) coefficient capacitors (an example case for even delay elements).

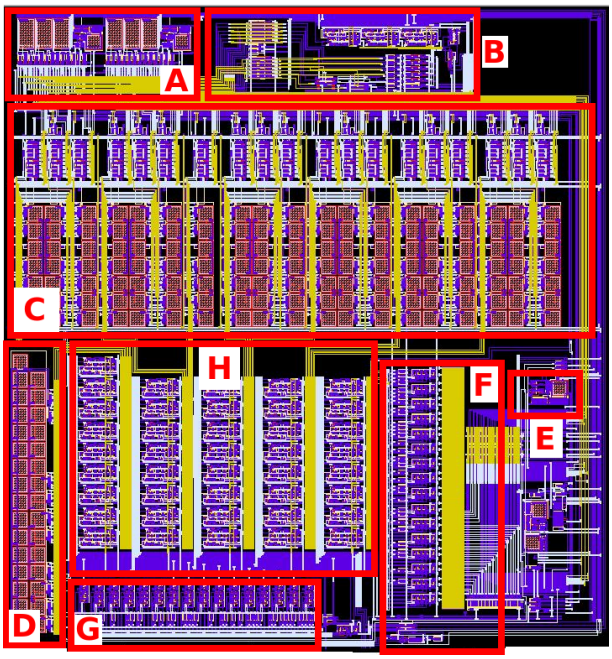

Fig. 2. Structure of the realized programmable filter. Main blocks include: (A) Even-Odd delay line, (B) multiphase clock generator, (C) programmable filter coefficients, (D) programmable capacitor, (E) operational amplifier, (F) I/O and control block, (G) address decoder, (H) memory block.

of such implementations and the ease of modifying the filter structure. It also enables the implementation of a filter with any frequency response, as coefficients may be unambiguously realized with any precision. In this case, however, the problem is a serial execution of particular operations such as multiplications, summation of signal samples, as well as rewriting of samples in the delay line. It is visible, in particular, in high order filters that contain several dozen or several hundred coefficients.

An alternative solution may be a hardware implementation of the FIR filters (the same for the IIR filters) [1], [3], [19]. With an appropriate approach the operations described above may be performed in parallel. Such possibilities are offered, for example, by filters implemented in field programmable gate arrays (FPGAs) or realized as specialized chip (ASIC – application specific integrated circuit). An example of the latter are analog SC FIR filters, which are subject of this work.

Parallel signal processing takes place here at all data processing stages, although details depend on the used hardware architecture of the filter. The delay line may be constructed in such a way that all sampling operations between the delay elements are performed in parallel. After the samples are rewritten, they are multiplied by the filter coefficients, which is also performed in parallel for all signal samples. Finally, the summing operation of the multiplication products is also performed in parallel.

SC FIR filters can be implemented in various ways [10], [11], [19]. Since they are analog solutions, the main problems in this case are the distortions resulting from copying samples between the capacitors in the delay line and between this line and the block of the filter coefficients. Rewriting errors can strongly affect the frequency response of the filter. Discrepancies are usually visible in the stopband, which may suffer from reduced attenuation in the comparison with theoretical values.

Another problem is a linear dependence between the capacitance values in the multiplier block and the values of the filter coefficients. With more selective filters, due to the large spread between coefficients, this may lead to very large capacitors. This impacts the chip area and data processing rate. With an appropriate approach, the described problems may be strongly limited. One of the possibilities is to decompose the filter transmittance into several sections connected in series. In this case the spread between coefficients is strongly reduced. We applied this solution successfully in our previous projects.

III. An Overview of the Filter Structure

A family of the SC FIR filters offers various structures. The main issue is the number of the operations of rewriting signal samples, which impacts the frequency response of the filter. In some approaches (e.g. the Gillingham filter), the number of these operations equals the filter order. However, such structures require relatively simple controlling clock [4]. There are also solutions, in which the number of the rewriting

operations does not exceed three, regardless the filter order (e.g. circular memory and rotator filters). In this approach, however, the control clock is much more complex, as the number of clock phases linearly depends on the order of the filter [7]. The development of microelectronics and the consequent miniaturization, however, causes that the implementation of even complex clock generators is not a big problem at present [18].

In this work we present a transistor level implementation of an even-odd SC FIR filter, which is a compromise solution between the two mentioned features. The delay line in such filters allows for reducing the number of rewriting operations of the samples, while the clock generator still features a relatively simple structure. Diagram of the filter and its particular components are shown in Fig. 1.

We have implemented the even-odd SC FIR filters in several CMOS technologies [4], [5], [6], [8]. The first filter of this type was implemented in the CMOS 0.8 μm technology, for the application in the GSM telephony [4]. In this case the filter coefficients had fixed values, as the main objective was to obtain a good match with the theoretical frequency response.

In this work we present another filter from this family. The structure of the designed chip realized in the CMOS 0.35 μm technology is shown in Figure 2. The silicon area equals 0.5 mm^2 (700$\times$700 μm). Main components, shown in Figure 2, are as follows [5]:

A. delay line composed of two (even and odd) delay elements. The delay components may be set up to store two or three samples, so that the 4^{th} or 6^{th} order FIR filter may be obtained. This approach increases the educational possibilities of the chip.
B. multiphase, reconfigurable controlling clock generator, with the number of clock phases dependent on the configuration of the delay elements (4 or 6 phases).
C. programmable matrix of the coefficient capacitors (CCs) and configuration switches (transmission gates). The capacitors are composed of, the so-called, unit capacitors (UCs). Each CC contains three sections with 1, 2 and 4 UCs, respectively. The configuration switches allow to use the CCs as positive or negative filter coefficients. As a result, the CCs offer values -7, -6, . . . , 0, 1, 2, . . . 7 UCs. The described features allow to program the frequency response of the filter.
D. capacitor used in the feedback loop of the operational amplifier (OA) in the summing block,
E. two stage OA, used in the summing block,
F. control block used to configure the chip, so that different tests may be performed,
G. address decoder,
H. memory block that stores the configuration settings of the chip.

The chip is controlled / tested by 15 external pins divided into three groups: (i) digital, control and programmable signals (8 pins), (ii) analog I/O pins used to test the filter performance (3 pins), (iii) power supply lines (4 pins).

IV. Measurement setup

The chip offers wide spectrum of tests and experiments due to the possibility of programming it in many ways. A configuration of the chip is stored in the internal RAM memory, so the programming should be performed after each power start-up, using a special programming sequence. The programming sequence, besides the configuration of the chip, setting values of the filter coefficients and capacitors, allows for testing the entire filter and also the individual components of the chip. The programming sequence is presented in Table I and the working modes of the chip — in Table II [5]. It is worth to notice that the addresses in the programming sequence change in the Gray code (only one bit is changed in one programming step). Therefore the programming is self-clocked (it does not need any additional clock signal).

TABLE I
Chip programming sequence

Address	States
0000	Neutral state
1000	Mode of the chip
1001	Mode of the filter (delay elements order R = 1 / R = 2)
0001	Filter coefficient: 1
0011	Filter coefficient: 3
0010	Filter coefficient: 2
0110	Filter coefficient: 6
0100	Filter coefficient: 4
0101	Filter coefficient: 5
0111	Filter coefficient: 7
1110	Output capacitor (after this MSB b5 = 1)
1110/ 1101	Output capacitor MSB b5 = 0 Output capacitor MSB b5 = 1
1100	External clock mode

TABLE II
Configuration modes of the chip

Mode	Description
1	All internal blocks are connected in the SC FIR filter
2	Measurement of the delay line
3	Measurement of the transmission gate
4	Measurement of the output capacitor
5	Measurement of the S&H delay element
6	Measurement of the OA
7	Measurement of the clock phases: n1, p1, n2
8	Measurement of the clock phases: n1, n2, n3
9	Measurement of the clock phases: p1 ,p2, p3
10	Measurement of the clock phases: n12, n23, n34
11	Measurement of the clock phases: n135, n246, p246
12	Measurement of the clock phases: p12, p23, p34

The chip, to work correctly, needs both digital and analog signals. The analog signals are input and output signals, e.g. of the filter, so the analog interface must produce input signals and measure the output signals. The digital interface must program the filter and produce clock signals.

For internal clock mode the chip needs two clock signals, for the external clock mode 4 or 6 (depending on the filter working mode). Because the programming is performed only once after the power-up, it may be performed with relative low speed. The clock signals, on the contrary, are much faster and

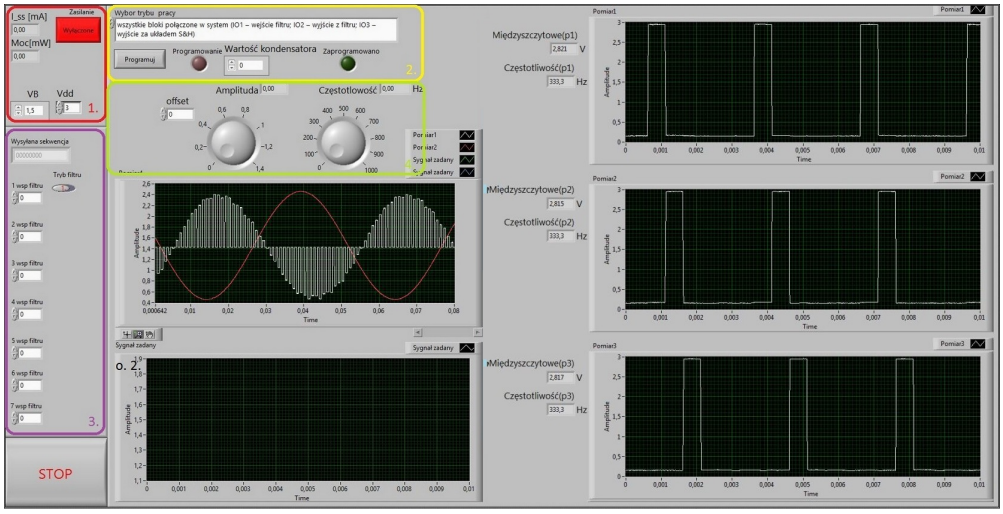

Fig. 3. Interface of the LabVIEW program used to test the designed chip.

should be delivered all the time and be very accurate. This is a common property of SC structures, that the quality of signal processing strongly depends on the accuracy of clock signals. Additionally, it is possible to tune the SC filters by changing the frequency of clock signals.

The interface for controlling of the chip was prepared with the use of two platforms: National Instruments CompactDAQ with LabVIEW environment and Altium NanoBoard NB2 FPGA evaluation board.

The software prepared in the NI LabVIEW 2015 environment [16] (presented in Fig. 3) offers programming of the chip (Fig. 3, frames 2 and 3), generation of the chip input signals (Fig. 3, frame 4), gathering of the chip output signals, visualization (virtual oscilloscopes), and automatic measurement of all processed signals (Fig. 3, frames 1 and 5).

The analog signals are produced via NI9263 digital-to-analog converter (DAC) module. This module has 4-channels, 16-bit resolution, 100 kS/s/ch sampling rate, and ± 10 V voltage range [14]. Using the software the user can modify the amplitude and frequency of the generated sinusoidal source signals (Fig. 3, frame 4). Two of analog output channels are used to control the powering of the chip, where the user can digitally set the DC voltages (Fig. 3, frame 1).

Actually, the chip is powered via DAC controlled L2722 1 A output current power amplifier from STMicroelectronics [20]. Beside the controlling of the supply voltages, the software measures the supply current and calculates the supply power.

The output signals, supply voltages and currents are acquired by NI9215 analog-to-digital converter (ADC). The NI9215 is 4-channel converter with 100 kS/s/ch sampling rate and ± 10 V output voltage range [13].

The signals for programming of the chip are generated in the LabVIEW software and interfaced to the chip via NI9401 digital 8-channel I/O TTL-level card [12] and two 74LVX125 digital level translators [9]. Because the powering voltage can vary, the digital signals must be controlled to be equal or lower than the powering voltage. All NI cards are placed in the CompactDAQ chassis NI cDAQ-9172, which is connected to the PC through USB port [15].

Multiphase clock signals are precisely generated in the second platform, namely the Altium NanoBoard NB2 with Xilinx Spartan3 FPGA chip [2]. To produce properly synchronized complementary clock signals we used FPGA-based programmable divider, which is clocked by the board source clock with controlled frequency from 6 MHz up to 200 MHz [2]. The divider produces clock signals, which are connected to the tested chip. These signals have exact 50% pulse width with frequency range from 300 Hz - 10 kHz. In fact, the chip can work with clock frequencies up to several MHz, but according to the sampling rates of the analog interface part, the signals with frequencies higher than 50 kHz may not be correctly sampled (in the SC circuits the analog signals are processed with sampling clock frequencies and this chopping process is visible on the output analog signals, cf. Fig. 4 (a), (b) and Fig. 5 (a), (b)).

V. Measurement results

In this section we present selected results of the laboratory tests of the chip [17]. We verified the correctness of the operation of particular filter components, the programming abilities and the behavior of the filter for different transfer functions.

Fig. 4 demonstrates performance of the filter in the lowpass mode, for the sampling rate of 1 kS/s. The consecutive filter coefficients were set to 0; 1; 3; 7; 3; 1; 0. Diagrams (a) and (b) present time domain results for the signal in the bandpass (20 Hz) and stoband (450 Hz), respectively. The overall frequency response of the low-pass filter is illustrated in diagram (c), for two modes of the filter operation (cf. Table

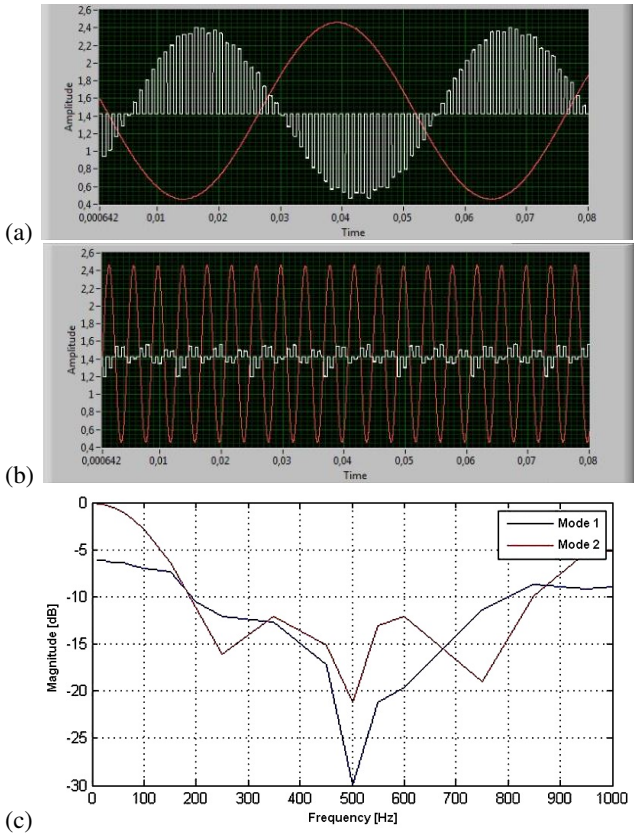

Fig. 4. Performance of the filter in the lowpass mode: (a, b) in time domain for passband and stopband, respectively, (c) frequency response.

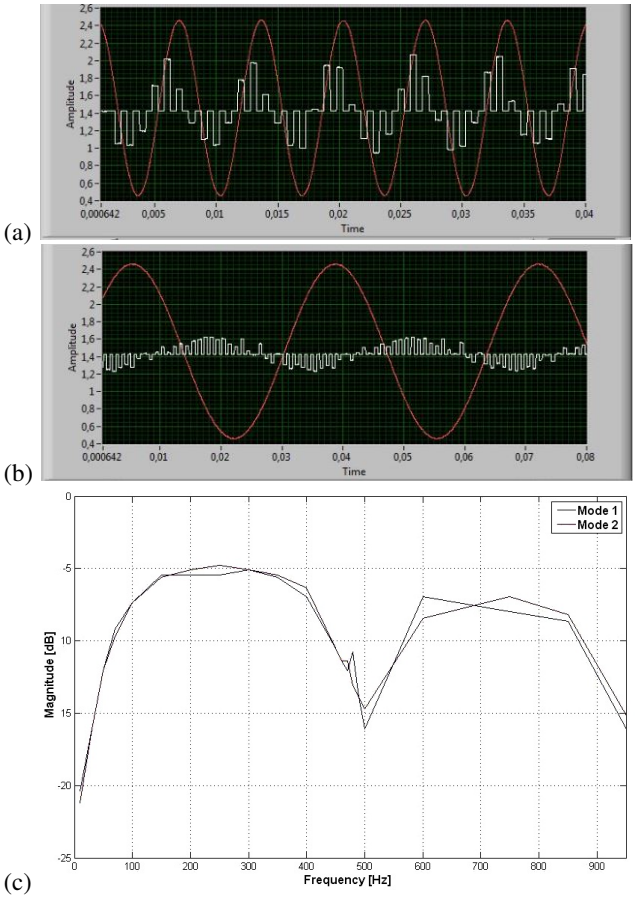

Fig. 5. Performance of the filter in the bandpass mode: (a, b) in time domain for passband and stopband, respectively, (c) frequency response.

I Mode of the filter). In the first mode the filter uses delay elements with order $R = 1$ (it has more, but less complicated delay elements). In the second mode the filter uses delay elements with order $R = 2$ (it has less, but more complicated delay elements).

Please notice that the filter order is just 6, so the length of the passband is relatively high and the attenuation is not higher than 25 dB. The frequency response is in average symmetric due to the digital nature of the SC FIR filter structure.

In both cases the bandwidth is in the frequency range 10–250 Hz. The attenuation in the stopband equals 25 dB and 20 dB in the 1st and 2nd mode, respectively. For the signal frequencies above 500 Hz, a typical reflection of the frequency response is visible.

Similar results for the bandpass mode are shown in Fig. 5. In this filter, the consecutive filter coefficients were set to 3; 5; 7; 7; 5; 3.

Fig. 6 illustrates selected measurement results of the controlling clock. One of the main issues during the design of this block was to obtain a very precise crossing point of two adjacent clock phases. Crossing a near to zero voltage is essential from the point of view of the filter behavior.

The clock generator works properly. The results on particular diagrams of Fig. 6 are shown for different sampling rates.

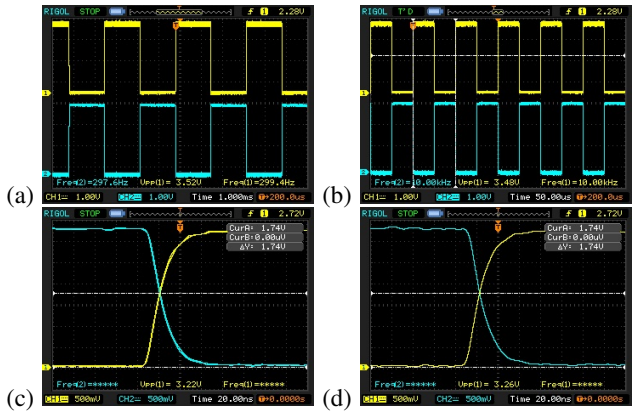

Fig. 6. Clock signals.

The most important for the SC circuits is synchronization of complementary phases: the falling and rising edges must cross just in the middle of the voltage range. As it can be seen in Fig. 6, the crossing is just in the middle, regardless the clock frequency. This ensures the best performance of the filter.

VI. Conclusions

The experiments shown that the filter programming procedure and filter modes operate correctly. The chip can be used for laboratory experiments in various university electronics courses starting with the basic course (investigation and measurement of basic elements and building blocks) and finishing with advanced courses devoted to the design of mixed analog-digital ASIC's, and to realization and programming of adaptive and programmable FPGA structures, or to the design of control and telecommunication systems, etc., in which the entire SC FIR filter will perform the necessary signal processing.

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