A 10-phases programmable clock generator for the application in control of SAR ADC realized in the CMOS 130 nm Technology

Rafał Długosz, Tomasz Talaśka
UTP University of Science and Technology, Faculty of Telecommunications, Computer Science and Electrical Engineering, ul. Kaliskiego 7, 85-796 Bydgoszcz, Poland
Email: rafal.dlugosz@gmail.com, talaska@utp.edu.pl

***Abstract*—In this paper we present a 10-phases programmable clock generator for the application in control of Successive Approximation Register (SAR) Analog-to-Digital Converters (ADC), realized in the CMOS 130 nm technology. The circuit provides 10 clock signals on separate terminals (sections). The programmable feature means that we can program the number of clock phases which are cyclically repeated. The circuit allows also to select which sections are used at the moment. For example, in case if only 6-phases are needed, we can obtain them on terminals 1-6, 2-7, ..., 5-10. This feature is important looking from the point of view the SAR ADC, in which corresponding branches can also be selected in the same way. The clock generator allows to control the width of the clock phases, which is also a useful feature.**

***Index Terms*—Clock generator, SAR ADC, Programmable Circuits**

I. Introduction

Multi-phase clock generators implemented inside the chip allow to reduce the number of pins of the chip, and therefore are very useful and commonly used. Such circuits are usually implemented using a chain of D-flip flops (DFFs) [1], [2], [3], [4], [5], [6], however other solutions are also in use. The advantage of solutions implemented on the basis DFFs is their simplicity and stability of their parameters. However, since a typical DFF is usually composed of 26 transistors, in case of large number of clock phases, the chip area becomes large. Such solutions also consume relatively large power. In multiphase clock generators, in a given time moment, the value '1' is usually at the output of only a single DFF. However, the CLK (clock) signal that controls the DFF switches over some gates in the DFF even if this circuit does not change its state. These gates are switches over two times, during rising and falling edges of the CLK signal.

In this paper we propose a clock generator which is based on the chain of NOT gates and switches. In this case the logical values are stored in the parasitic capacitors of the NOT gates that serve as short-time memory cells. The structure of the generator has been extended to obtain the ability to program the number of phases, as well as to enable selection of the sections which are used at the moment. This feature is important looking from the point of view of the application of the circuit. It has been designed to provide signals that control particular conversion stages in a successive approximation register (SAR) analog-to-digital converter implemented in the CMOS 130 nm technology.

The paper is organized as follows. In next Section we present the structure of the proposed circuit. In the following Section selected simulation results are provided. The conclusions are drawn in Section IV.

II. The proposed clock generator

The proposed circuit is shown in Figure 1. It is composed of a chain of 10 blocks denoted as ICLK_ATOM and an 9-inputs OR gate. The structure of the first block in the chain (ICLK_ATOM_IN) is different than of the ICLK_ATOM, as this circuit plays a different role. The structures of both circuits are shown in Figs. 2a and 2b, respectively. The overall clock generator is controlled by a 2-phases external clock (terminals clk1 and clk2).

A general principle of operation of the realized circuit is as follows. The situation in which there is no logical '1' signal at the output of at least one of the ICLK_ATOM blocks is prevented by the use of 9-inputs NOR gate. In case if all inputs of the NOR gate are equal to '0', the gate generates a new '1' signal, which is provided to the chain, and then propagated between subsequent ICLK_ATOM blocks, according to following clk1/clk2 pulses. Each ICLK_ATOM block provides complementary 'Nclk$x$' and 'Pclk$x$' signals, which are directly the clock phases, used to control switches in the ADC. The switches are designed as transmission gates, composed of NMOS and PMOS transistors, and thus the complementary signals are required.

The role of the ICLK_ATOM_IN block is to provide the generated '1' signal (CLK1st_out) to one of the selected ICLK_ATOM blocks. For this reason the output of this block is connected to all ICLK_ATOM blocks in parallel. The selection of a given ICLK_ATOM block that will by able to use this signal as a first in the chain, is programmed using a sequence of the Bsi9 - Bsi0 bits. To explain it in detail, let us consider an example 1011111011 (Bsi9 – Bsi0). The Nclk$x$ signal can be activated only if the OR gate in a given x^{th} ICLK_ATOM block is able to generate '1', which is

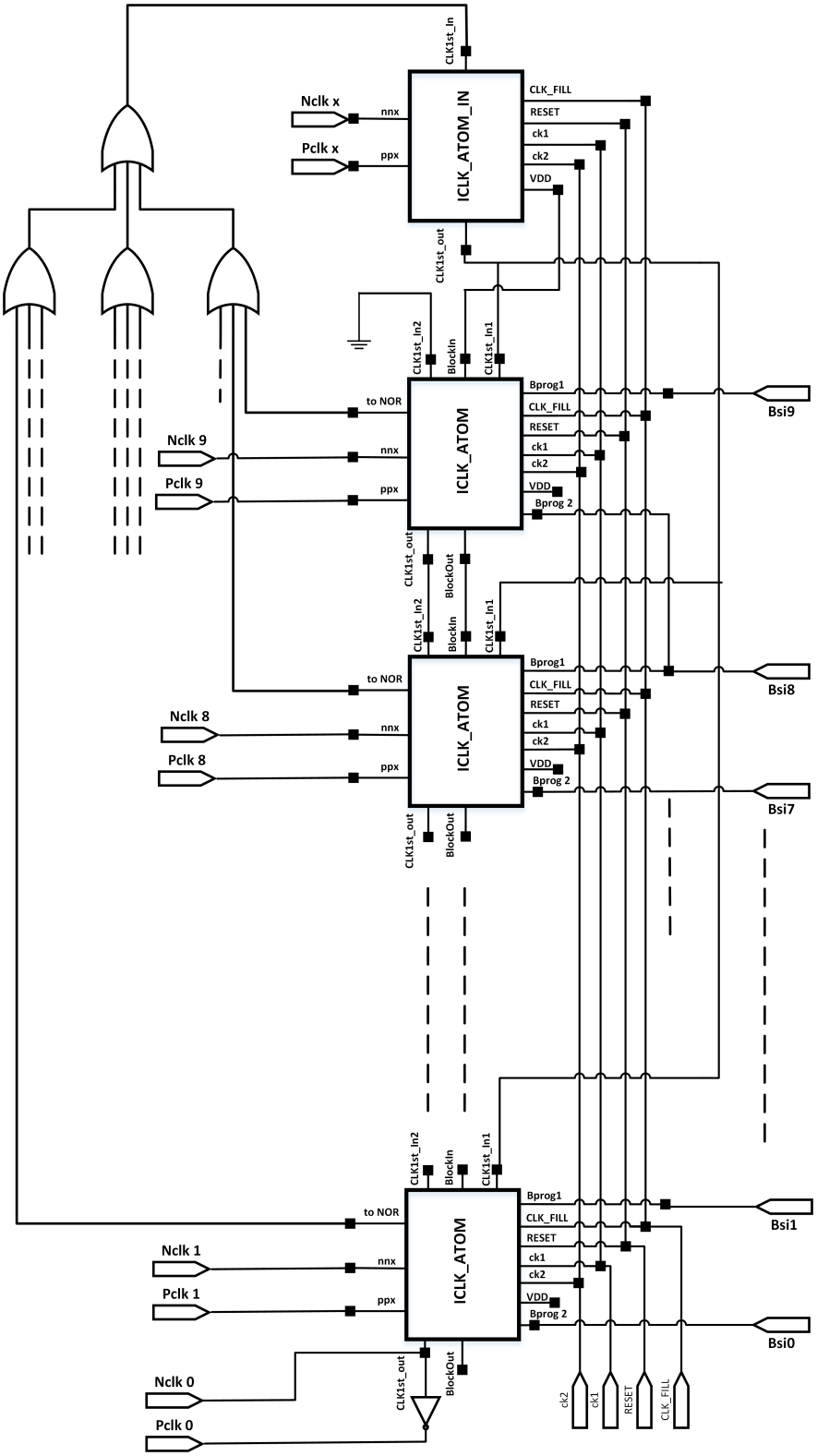

Fig. 1. General structure of the proposed 10-phases clock generator.

possible if the chain of the NOT1-AND1-AND5 gates provides '1' or if the CLK1st_in1 signal is '1'. On the other hand, the CLK1st_in1 signal can be '1' only if a given Bprog$x$ signal (in Fig. 1) is '1' (in this case the AND2 gate of the

preceding section can generate 1). The BlockIn signal of the first ICLK_ATOM is permanently connected to VDD, while the CLK1st_in2 of the first ICLK_ATOM is connected to the ground. In this example the MSB (Bsi9) equals '1'. For this reason, the in1 terminal of the OR gate is '0'. Since the in2 terminal of the OR gate is also '0', the 1^{st} section is unable to generate the Nclk9 and Pclk9 clock phases. In the consequence the output of the AND2 gate is always '0' in this case, i.e. the in2 terminal of the OR gate in the next (8^{th}) ICLK_ATOM block is also '0'. The Bsi8 signal is '0' in this example. As a result, the in1 terminal of the AND1 gate in the 8^{th} section equals '1'. The in2 terminal of AND1 is also '1', as the BlockIn signal is still '1'. The in3 terminal of AND1 is '1', as the ICLK_ATOM_IN provides such signal to all ICLK_ATOM sections. As a result, at the output of the OR gate in the 8^{th} section we have '1', and this section is able to generate its Nclk8 and Pclk8 clock phases. Since the next five Bsi$x$ signals are '1', the outputs of the AND2 gates in the corresponding sections can be '1', i.e. the clock generator can generate the corresponding clock phases. However, since Bsi8$=0$, therefore all BlockIn signals in subsequent sections are blocked by their AND5 gates, and the outputs of all AND1 gates of these sections are also '0'. In this situation the only possibility to generate the Nclk$x$ and Pclk$x$ phases is if the in2 terminals of the OR gates are '1'. This possibility is blocked by the second occurrence of '0' at one of the Bsi$x$ terminals.

Summarizing, generation of the clock phases starts at this section at which there is the first occurrence of the '0' value, and ends at this one at which there is the second occurrence of the '0' value. To reprogram the circuit it is necessary to modify either 2 or 4 bits only.

Particular Nclk$x$ and Pclk$x$ signals are generated at the output of the AND4 and NOT5 gates located in the ICLK_ATOM sections. Each clk1/clk2 sequence moves the '1' signal from the OR gate on one section to the next one throughout the chain of the switches SWITCH1, SWITCH2 and the NOT2, NOT3 and AND2 gates. To obtain a proper width of particular Nclk$x$ and Pclk$x$ signals the in2 terminal of the AND4 gate obtains an appropriate CLK_FILL signal. A separate signal (not dependent on the CLK_FILL signal) is provided throughout the AND3 gate to the 9-inputs OR gate shown in Fig. 1. Those ICLK_ATOM sections which are inactive, are unable to provide the '1' signal to in1 terminal of their AND3 gates, so they remain neutral.

III. Verification of the Proposed Circuit

The circuit has been verified by means of the postlayout simulations performed in the Spectre environment. In this Section we present selected results for different programming sequences and different CLK_FILL signals, to illustrate the flexibility of the proposed circuit.

Fig. 3 illustrates the results for all clock phases being active. The programming sequence of Bsi9-Bsi0 bits is in this case equal to '0111111111', i.e. the second occurrence of the '0' signal does not appear. The results are shown for three different shapes of the CLK_FILL impulses. The resultant

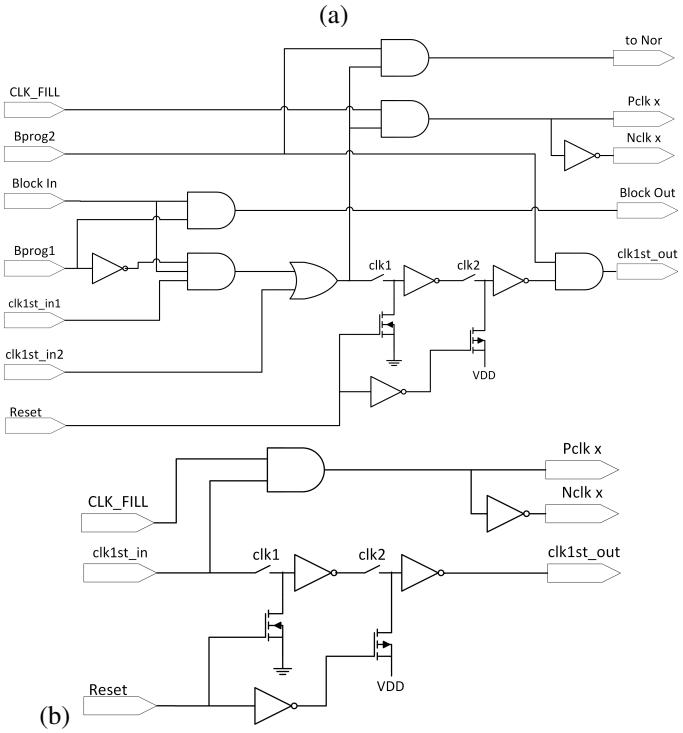

Fig. 2. Diagrams of the (a) ICLK_ATOM and (b) ICLK_ATOM_IN sections used in the clock generator

clock impulses have different widths. The results are shown for Nclk$x$ signals used to control NMOS transistors in the transmission gates. This feature allows to control precisely the crossing moments between two adjacent clock phases, which has a strong impact on the control of the glitches that can occur in the ADC. The clock generator can be reset at any time by the use of the Reset signal provided directly to the gates of the NMOS transistors in the ICLK_ATOM and ICLK_ATOM_IN blocks. The same signal, after negation in the NOT4 element is also provided to the gate of the PMOS transistor. In the presented results, the Reset signal is activated about 420 ns. After this time the clock cycle is repeated, starting with the first allowed phase.

Fig. 4 illustrates similar results for the programming sequence of '1111011110'. Since only the Bsi5 signal is set to '0', the nclk9 – Nclk6 phases are inactive. The next phases Nclk5 – Nclk1 are active, while the Nclk0 is deactivated by the '0' signal at the Bsi0 terminal. The results are shown for two example CLK_FILL signals.

One of the important parameters is the power dissipation of the circuit which can be assessed on the basis of the supply current (I_{DD}). The current spikes occur during switching over the circuit, so the numbers have to be averaged. Fig. 5 shows selected results for the '1111011110' mode. However, the results do not depend strongly on the number of the active phases. In those sections that do not carry the '1' signal at the moment, there is no switching of the logic gates, so these sections do not contribute substantially to the overall power

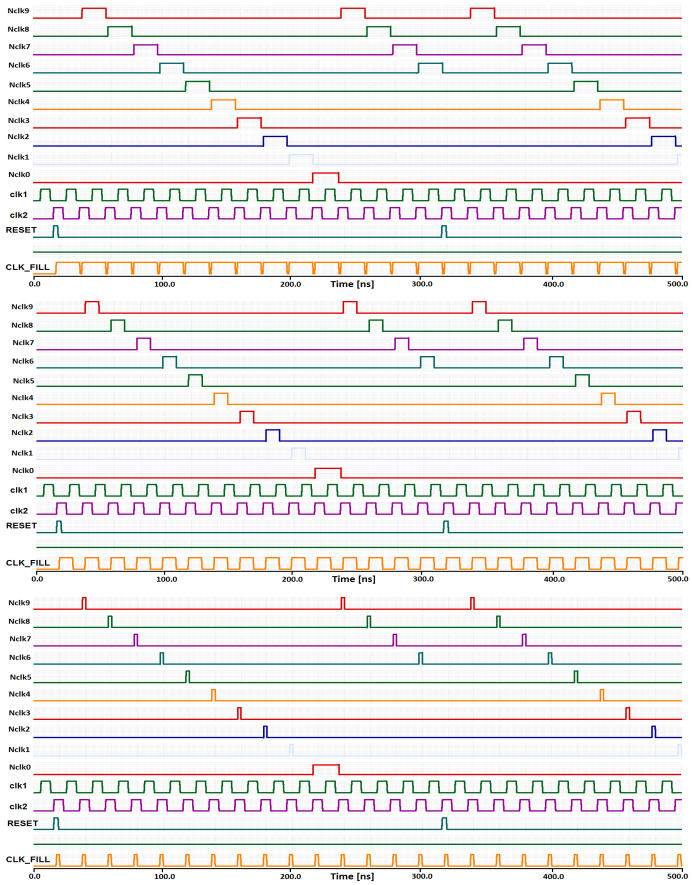

Fig. 3. Waveforms for all clock phases being active (mode '0111111111'), for different widths of the CLK_FILL impulses.

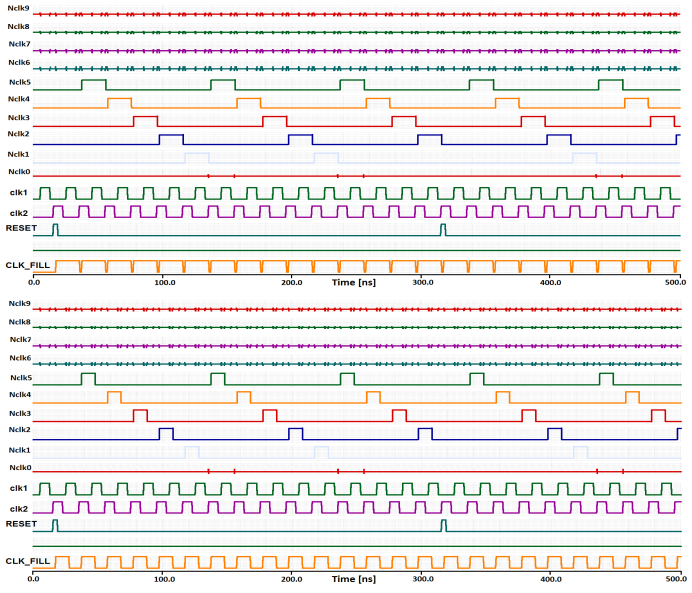

Fig. 4. Waveforms for only 5 clock phases being active (mode '1111011110').

dissipation of the clock generator. For the worst case (the largest spikes), an average energy consumption per a single

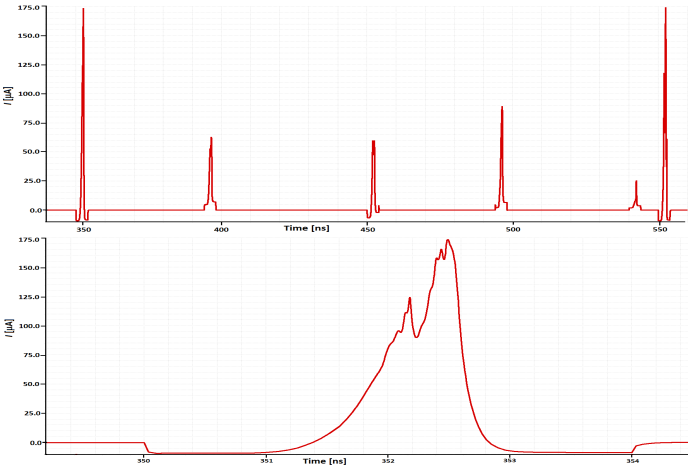

Fig. 5. Supply current.

clk1/clk2 cycle approximately equals 145 fJ. In the comparison with the solutions based on DFFs the obtained results are much smaller.

IV. Conclusion

In this paper we present a novel flexible clock generator realized in the CMOS 130 nm technology. The circuit ha been designed as 10-phases, however, any extension is possible by simple duplication of the ICLK_ATOM blocks connected in chain.

The circuit is programmable, which means that we can obtain any number of the clock phases, and additionally we can program which sections are active. This feature is useful in the target application as control block for the programmable SAR ADC [7]. The width of the clock impulses can be also easily changed.

References

[1] X. Gao, E. A. M. Klumperink, B. Nauta, "Low-Jitter Multi-phase Clock Generation: A Comparison between DLLs and Shift Registers", *IEEE International Symposium on Circuits and Systems* (ISCAS), 2007, pp. 2854-2857

[2] C. C. Liu, S. J. Chang, G. Y. Huang and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure", *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, 2010, pp. 731-740

[3] R. Dlugosz, P. Pawlowski and A. Dabrowski, "Multiphase clock generators with controlled clock impulse width for programmable high order rotator SC FIR filters realized in 0.35 m CMOS technology", *Proc. SPIE 5837, VLSI Circuits and Systems II*, 1056, 2005

[4] D. Shin, J. Koo, W. J. Yun, Y. Choi and C. Kim, "A fast-lock synchronous multi-phase clock generator based on a time-to-digital converter", *IEEE International Symposium on Circuits and Systems*, (ISCAS), 2009, pp. 1-4

[5] Li Dong, Meng Qiao and Li Fei, "A 10 bit 50 MS/s SAR ADC with partial split capacitor switching scheme in 0.18μm CMOS", *Journal of Semiconductors*, vol. 37, no. 1, 2016, pp. 015004

[6] C. N. Chuang and S. I. Liu "A 40GHz DLL-Based Clock Generator in 90nm CMOS Technology", *IEEE International Solid-State Circuits Conference*, (ISSCC), 2007, pp. 178-180

[7] R. Dlugosz, G. Fischer, "Low Chip Area, Low Power Dissipation, Programmable, Current Mode, 10-bits, SAR ADC Implemented in the CMOS 130nm Technology", *International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, (June 2015), pp.348-353