A Low Power, Low Chip Area Decimation Filter for $\Sigma - \Delta$ Modulator for Flywheel MEMS Gyro realized in the CMOS 180 nm Technology

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Abstract—**The paper presents a low power and low chip area decimation filter for a 15-bits $\Sigma-\Delta$ analog-to-digital converter (ADC) designed for a flywheel MEMS gyroscope. In contrary to typical solutions, in which decimation is performed after each filtering stage, in the proposed approach all filter sections operate at the sampling frequency of the modulator. The low power dissipation is in this case achieved by substantially simpler structure of particular stages. By selecting the oversampling ratio (OSR) of the modulator sufficiently large, e.g. 200, the decimation filter composed of Finite Impulse Response (FIR) filters with equal coefficients does not distort the passband signal. The low chip area results from eliminating a complex selective filter usually placed at the end of the filtering chain in the decimation filter.**

I. Introduction

Requirements of modern circuits force to design systems with low power consumption and small size. When it comes to ASIC realization complexity and number of transistors are important issues of the final design. Hence, any modification of widely used solution that improves the design in terms of the mentioned above criteria is worth to consider. In this paper a new approach to the decimation filter is proposed. Such filters are key blocks in any oversampled A/D converters. Taking into account the area and power used by oversampled A/D, such filters usually take most of the power and occupy a large chip area. Decimation transforms the digitally modulated signal from short words occurring at a high sampling rate to longer words at the Nyquist rate while suppressing much of the high frequency quantization noise. Usually it is a 1-bit data stream with a high frequency sampling.

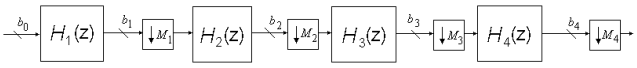

Fig. 1. A typical multistage decimation filter used to remove the quantization noise in the oversampled ADC.

A typical cascade structure of the decimation filter is shown in Fig 1. Particular approaches reported in the literature differ in the structure of particular stages (H1(z) ... H4(z)). Many approaches were proposed starting with as simple as a counter up to different cascade structures based on comb filters. One of such solution is proposed in [1]. The decimation process is in this case divided into three stages. The first stage is realized as a CIC (Cascaded Integrator Comb) filter, which does not require a multiplier. However, because of a magnitude drop in the pass-band the second stage, the FIR filter, is required to compensate this characteristic. Finally, the last stage is a half-band FIR filter. This solution minimizes the number of required multiplications that, in turn, minimizes the chip area and the power consumption.

In general, in all reported solutions the optimization efforts of the filter structure rely on minimizing the number of the multipliers and/or on minimizing the number of multipliers that operate at high frequencies. This is the reason why in typical solution the first stages that operate at high frequencies are usually simple, while the last stage that operates close to the Nyquist frequency is a complex "narrow" filter.

In this paper we propose another solution of the decimation filter. The filter is also composed of several stages (three in this case) but the decimation factors after particular stages ($M1$, $M2$ and $M3$) equal one, i.e. there is no decimation between intermediate stages. A disadvantage of this approach is that all these stages operate at high clock frequency equal to the sampling frequency (f_S) of the modulator. To make this problem

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insignificant all these stages are very simple FIR filters of order $N = 31$ or 15 with equal coefficients, so that they do not require multipliers. As a result, although the filter operates at high frequency but the power dissipation is relatively low. An additional advantage of this solution is a very low chip area, which is one of the paramount features in the system in which the ADC will be used. The $\Sigma - \Delta$ ADC with the proposed decimation filter is to be used as a component of high precision 6 degrees of freedom flywheel MEMS gyroscope. The overall system is composed of six independent control loops, each containing a separate ADC. This is one of the reasons why the structure of a single ADC has to be very simple.

II. The proposed decimation filter

The proposed filter is composed of equal sections that differ only in the number of bits in particular signals. An example block diagram for the 1st section is shown in Fig 2. In this case the input signal is a 1-bit stream directly coming from the modulator, while the resolution at the output of this section equals 5 bits. Each section requires only one multi-bit full adder, one multi-bit full subtractor, a delay line (shift register) composed of 31 delay elements, T, and a simple accumulator (digital memory). As a result, the overall decimation filter requires only 6 multi-bit adders and subtractors, while the total number of transistors in case of $N = 31$ (15 bits at the output) does not exceed 6500. In the CMOS 180 nm technology the chip area of the overall filter equals about 0.05 mm^2.

Particular sections operate as follows: The sum of all $N+1$ samples of the delay line is stored in the accumulator. For particular signal samples entering the filter this sum is updated by adding a new sample entering the delay line and subtracting the one that leaves the filter. This requires only two operations. One of the advantages of this approach is that the filter calculates in this way all output samples, so that the decimation at the output of the ADC can be performed by any factor M, which makes such solution more flexible. This is in contrast to solutions based for example on counters, in which decimation after particular sections has to be performed by the factor equal to the length of particular sections.

A. Analysis at the system level

An important question is if such filter assures a sufficient noise rejection at low sampling frequencies. The FIR filters with equal coefficients are rather poor filters, which means they are not very selective, especially at low signal frequencies close to passband. In the proposed solution we improved the attenuation of the overall decimation filter by connecting three sections with equal coefficients in series. As a result, we obtained the frequency response shown in Fig. 3 (top) (the $H_3(z)$ curve). The problem with this approach is that in parallel with improving the attenuation in the stopband we observe an increasing distortion of the signal in the passband, as shown in Fig. 3 (bottom). This problem can be reduced either be reducing the order of the filter or by increasing the oversampling ratio (OSR). For relatively high order $N = 31$ and an example $OSR = 100$, the distortion for the upper passband frequency (cutoff) does not exceed 4.5 dB (case A in Fig. 3 (bottom)). For $N = 31$ and $OSR = 200$ or for $N = 16$ and $OSR = 100$ the distortion is reduced to 1.2 dB only (case B), which is sufficient in case of the application of the filter in the gyro. For $OSR = 400$ (case C) and $OSR = 800$ the distortion is reduced to 0.4 dB and 0.1 dB only, but at the expense of very large power dissipation.

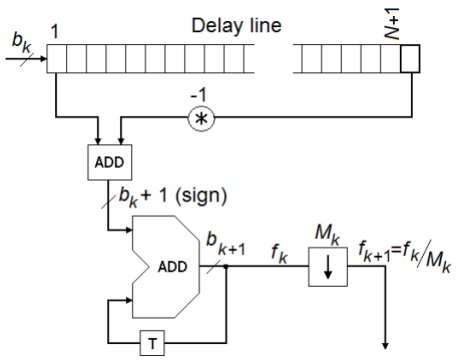

Fig. 2. The proposed FIR filter (with equal coefficients) used in particular stages of the decimation filter.

For the frequencies above but close to the cutoff frequency the attenuation at the output of the 3rd section is low (40 dB) but it is compensated by sufficiently large Signal-to-Noise Ratio (SNR) at the modulator output, which is due to noise shaping. The calculations show that for the 2nd order modulator, the SNR is sufficiently large to assure the noise rejection at the level of 100 dB in the overall frequency band (see Fig.4), i.e. more than required 15 bits that is sufficient to enable a proper closed-loop control of the gyroscope. Such numbers have been determined by means of detailed system level simulations of the model of the gyroscope.

An important parameter that has to be considered in the closed-loop control of the gyro is the group delay introduced by the decimation filter, which in this approach is located in the control loop. The investigations completed by means of the mentioned model of the gyro show that a delay of even 3 μs did not disrupt the system behavior. In case of using three sections of order $N = 31$ each and $OSR = 200$ (similar results are for $N = 15$ and $OSR = 100$) the group delay equals about 250 ns, i.e. the safety margin is sufficiently large. For $N = 31$ and $OSR = 100$ the group delay increases to about 500 ns. Selected system level simulations for large and small ADC input signals are shown in Fig. 5.

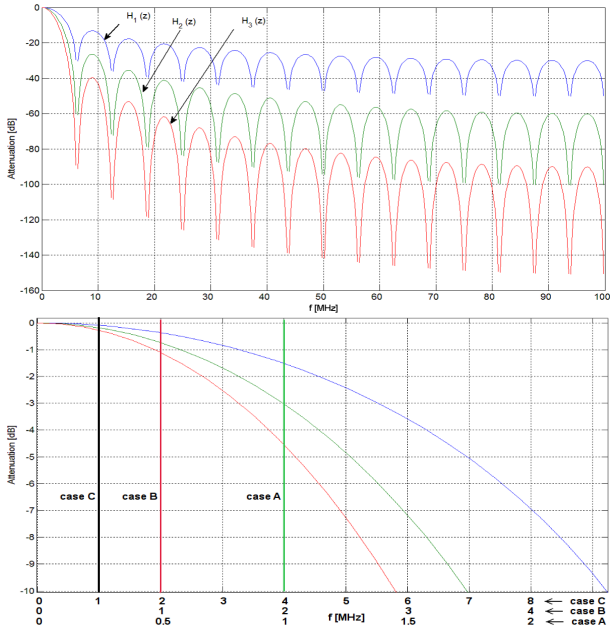

Fig. 3. Frequency response at the output of particular sections of the decimation filter (the $H_3(z)$ curve is for the overall filter), for the cutoff frequency of 1 MHz: (top) a general view for $OSR = 200$ (case B); (bottom) a comparison for different values of the OSR (cases A for 100, B for 200, C for 400).

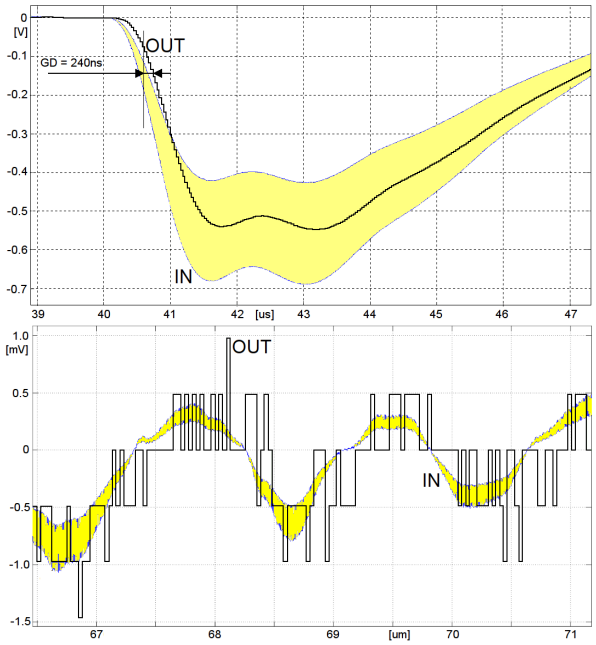

Fig. 5. ADC noisy input signal as well as the output signal after decimation by 4 (32 MSampl/s), for: (top) large and (bottom) small input signals. The results are shown for 3 filter sections of order $N = 15$ each (12 bits of the resolution). The modulator operates at $f_S = 128$ MHz.

The ADC input signal, varying in-between -1 and 1 V is accompanied by a noise (the yellow area). The results are shown for $OSR = 128$ ($f_{S(modul.)}$=128 MHz) and $N = 15$, i.e. for the resolution at the output of the ADC of 12 bits. The output signal is in this case decimated by a factor $M = 4$, i.e. $f_{S(out)}$=32 MHz.

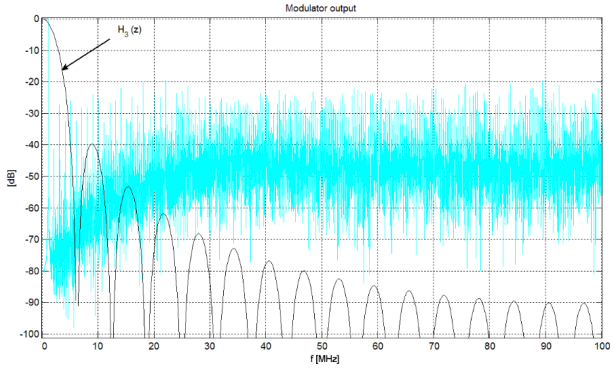

Fig. 4. Noise spectrum at the output of the modulator.

III. Implementation of the filter at the transistor level

The proposed decimation filter has been implemented at the transistor level in the CMOS 180 nm technology. An electrical diagram of the 1st section is shown in Fig. 6. The remaining two sections have similar structure, differing only by the resolution of particular signals. The delay line of the filter has been realized as a cascade connection of switches (transmission gates) and NOT gates, while the samples are stored across parasitic capacitances of particular NOT gates. This approach, in comparison with the realization based on a cascade connection of D-flip-flops, significantly reduces the power dissipation of the delay line [2].

All sections are programmable (signals FIR8, FIR16, FIR32). The available orders N are 7, 15 or 31, i.e. the available resolutions at the output of the ADC vary in-between 9 and 15 bits. The overall filter in the Hspice simulations consumes 10 pJ per a single calculated output sample, on average. The max achievable f_S equals 500 MHz, although f_S of 200 MHz is sufficient in the application of the filter in the gyro. It is worth noticing that if all sections are equal and operate at data rate of the modulator, the output signal can be decimated by any factor, which makes the proposed filter a very flexible solution. On the other hand, as in this case the output signal is decimated by at least $M = 100$, the last section can be substantially simplified and realized as a counter, without the delay line and the subtractor. The last section is the most complex (the highest resolutions of the signals) and such simplification will reduce the power dissipation even by 40 %.

Selected transistor level simulation results are shown in Figs.7 and 8. The supply current is shown for the worst case i.e. for large input signals that activate most of the logic blocks. Typical current spikes are much

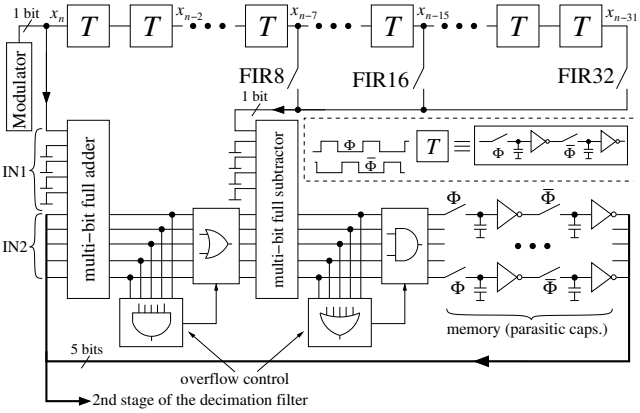

Fig. 6. Diagram of the proposed filter (the 1st section) with a programmable order N (available options: 7, 15 and 31).

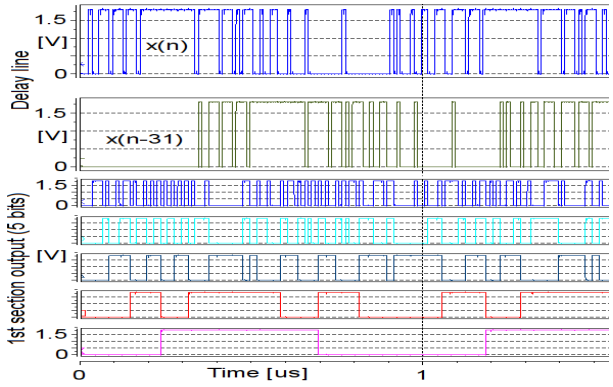

Fig. 7. Transistor level verification of the proposed filter: (top) a 1-bit output signal from the modulator – the 1st, $x(n)$, and the last, $x(n-31)$, sample stored in the delay line; (bottom) the signal at the output of the 1st section (for $N = 31$) of the decimation filter.

smaller, with an average energy consumption of about 4 pJ/sample. After the described simplification of the last section the energy will be further reduced.

A. Comparison of the parameters of reported filters

The comparative study of the parameters is shown in Table I. A direct comparison is not easy, as the power dissipation and the chip area are strongly dependent upon the structure of the filter, intermediate decimation factors, resolution of particular signals, process, supply voltage, etc. The presented data show that the proposed filter offers energy consumption close to the best state-of-the art solutions, while the chip area is more than one order of magnitude smaller. As mentioned earlier the energy consumption can still be minimized by simplification of the last section.

IV. Conclusions

A new low power and low chip area decimation filter for the $\Sigma - \Delta$ modulator has been presented. Due to simplification of the structure of the filter the chip area has been reduced to 0.05 mm^2, while the energy consumption is comparable with the best solutions of this type. The $\Sigma - \Delta$ ADC is to be used in the control loop of the high precision flywheel MEMS gyroscope.

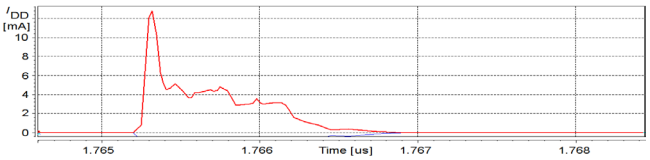

Fig. 8. Supply current during calculation of a single output sample at data rate of 500 MHz. For impulse width of about 1.5 ns, and an average current during this period of 3.6 mA, $E \approx 9.6$ pJ/sample.

TABLE I
Performance comparison between reported realizations of the decimation filter

Ref. (Techn.)	Res.	Area [mm]^2	f_S [MHz] (M)	P [mW] (pJ/S)
[2] (180nm)	6	ND	64 (4)	0.008 (0.1)
[3] (180nm)	16	0.15	1.28 (128)	21 (16nJ/S)
[4] (90nm)	16	ND	430 (16)	1.4 (3.25)
[5] (180nm)	24	1.86	11.3 (256)	2.35 (207)
[6] (0.6μm)	16	21*	32 (128)	490 (15nJ/S)
This work	9-15	0.05	200** (any)	0.8 (4)***

* The area includes analog modulator
** The maximum $f_S > 500$ MHz (Hspice simulations)
*** Average values for not simplified last filter stage

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