High-precision analogue peak detector for X-ray imaging applications

R. Dlugosz and K. Iniewski

A new analogue high-precision peak detector is presented. Owing to its very low power consumption the circuit is particularly well suited for photon energy detection in multichannel receiver integrated circuits used in nuclear medicine.

Introduction: Electronic signal detection and processing of X-ray images is gaining widespread acceptance owing to its inherent benefits of data storage and transmission in a digital format as opposed to conventional X-ray film [1]. One of the critical issues in signal processing is an accurate readout of signal amplitude that corresponds directly to photon energy [2]. A block diagram of a typical photon energy detection circuit used in a multichannel ASIC receiver is shown in Fig. 1. The peak detector (PD) is one of the critical blocks in this system as accurate X-ray photon energy is determined by the detected peak amplitude. Standard PDs may be sampled or asynchronous solutions. Sampled PDs are more precise but suffer from high circuit complexity and dissipate high power [3, 4]. Asynchronous PDs have simpler structure but suffer from lower output precision [5, 6]. The sampled PD proposed in this Letter is very precise and offers very low power dissipation. The proposed solution, as opposed to [6], has simple structure, where the delay line has only two memory elements. The gate-to-source capacitors (C_{GS}) are used as a short-term analogue memory, resulting in very small overall chip area in comparison to other sampled and asynchronous solutions.

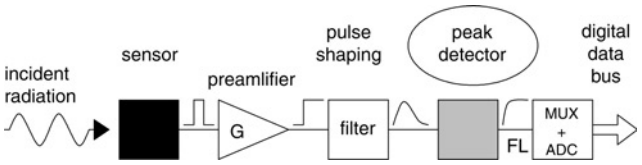

Fig. 1 *Photon energy detection circuit used in multichannel ASIC receiver*

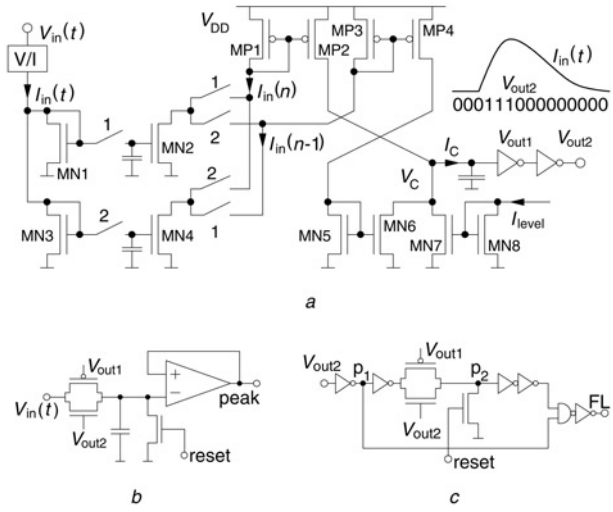

Fig. 2 *Proposed peak detector*

a Latching circuitry with switched current circular delay line and rotator switch
b Sample and hold voltage-mode circuitry
c Flag generation circuitry

Proposed peak detector: The proposed PD, which uses a novel current-mode latching mechanism and flag generation circuitry, is shown in Fig. 2. The primary function of the receiver circuit is to detect and amplify asynchronous pulses coming from the X-ray radiation sensor. The PD task is to catch the peaks of these pulses and to set an output flag (FL) requesting the receiver system to read out these peaks. The range of input pulse widths where the pulse is correctly captured depends on the frequency of the controlling clock signal f_{clk} and can be easily scaled up and down. For example, for the designed application of X-ray count rate of one million counts per 64-channel chip the desired f_{clk} is about 10 MHz and the impulse range can vary between 1 and 2 µs. The input pulse width is in turn controlled by a pulse signal filter (see Fig. 1) prior to signal detection [5]. One of advantages of the proposed circuit is that the two-phase clock signal does not need to be very precise in terms of its frequency stability as f_{clk} can vary even by 10% (for example, owing to temperature changes). As a result the clock generator can be fully integrated in the chip, without requiring an external stabilising quartz.

The proposed latching mechanism works as follows. The input voltage signal after conversion to current is subsequently sampled by a rotating delay line. The configuration of switches in the circuit shown in Fig. 2*a* causes the recent samples stored in the delay line to be copied to a comparator as a positive value through a PMOS-type current mirror, while the samples stored previously are copied to the comparator as a negative value, using the NMOS type current mirror. The comparator is realised using parasitic C_{GS} capacitances in the inverter. The important feature in the proposed solution is that the negative samples are strengthened by an additional current I_{level}, which may remain constant or be automatically adjusted during circuit operation, and can be treated as a parameter that controls timing precision and power of the latching mechanism. For all input samples the following relationship for comparator current I_C is always true:

$$I_C(n) = I_{in}(n) - I_{in}(n-1) - I_{level} \quad (1)$$

When the input signal is rising, the sample stored most recently is always larger than the previous one. Now, if the difference between both samples is larger than I_{level}, then the current I_C is positive, causing the comparator output V_{out2} to be a logical 1. Logical 1 to 0 transfer at the comparator output is expected when the peak of the input signal has been reached and the input signal starts to fall. When the input signal varies in a small range (some input noise is to be expected), I_C is also negative and the comparator output V_{out2} is also at logical 0 assuming that the I_{level} current is selected to be higher than the noise level. Current I_{level} protects the comparator against accidental switching over and losing the information stored in the sample and hold (S/H) element, when the input signal is noisy. This functionality can be expressed as:

$$V_{out2} = 1 \text{ for } I_{in}(n) - I_{in}(n-1) > I_{level} \quad (2a)$$

$$V_{out2} = 0 \text{ for } I_{in}(n) - I_{in}(n-1) < I_{level} \quad (2b)$$

Transistors sizes in the main circuit shown in Fig. 2*a* have been chosen as follows: MN1–MN4: 4/0.18 µm, MN5–MN8: 4/1 µm, MP1–MP4: 4/1 µm. The comparison voltage V_c is applied to the inverter input that serves as a comparator. The non-ideal behaviour of this element has no performance impact in the discussed application as the internal voltage crosses the V_c level rather quickly. In more elaborate implementation a true comparator with hysteresis can be used.

Two additional circuits interface with the latching mechanism. The first is a voltage S/H circuit, shown in Fig. 2*b*, which is controlled by the comparator outputs V_{out1} and V_{out2}. The second circuit used to generate a flag is shown in Fig. 2*c*. Parasitic capacitance at the node p_2 serves as a storage capacitor. The voltage at this point is a delayed copy of the output signal V_{out2}. When V_{out2} changes from logical 1 to logical 0 the switch will open, before the voltage at p_2 point flips from 1 to 0. As a result during the rising edge the voltage at p_2 tracks the output of the comparator, latching its value only when V_{out2} changes from 1 to 0. Signal p_2 cannot be used directly as a flag as its value is already 1 during the rising edge of the signal. The real flag (FL) is set to 1 when V_{out2} changes from 1 to 0.

The current mode S/H elements used in the delay line are not very precise circuits owing to charge injection effects. In the proposed latching mechanism these effects are of no consequence. This advantage results from the fact that the current I_C is equal to the difference between the samples stored in this two-element delay line. Consequently, even if charge injection is high (represented by the effective injection current I_E), the final expression for I_C does not contain the I_E term as indicated by

$$I_C(n) = I_{in}(n) + I_E - I_{in}(n-1) - I_E - I_{level} \quad (3)$$

To illustrate operation of the proposed circuitry, timing waveforms are shown in Fig. 3. A pulse width of 1 µs is used and $f_{clk} = 10$ MHz. The I_{level} causes the comparator to starting latching at the end of the rising edge, not after the peak value has been already passed, as in the solutions presented in [5] and [6]. In addition, the latching mechanism is very fast allowing the system to store the peak value very close to its real maximum. As a result the accuracy of the proposed peak detector is

very high, in particularly for quickly changing signals, better than 0.7% for a wide range of the input signal, as shown in Fig. 4. For higher input signal amplitudes accuracy is better than 0.25%. The circuit is capable of measuring peak amplitudes from 0.2 to 0.99 V (for a power supply V_{DD} of 1 V).

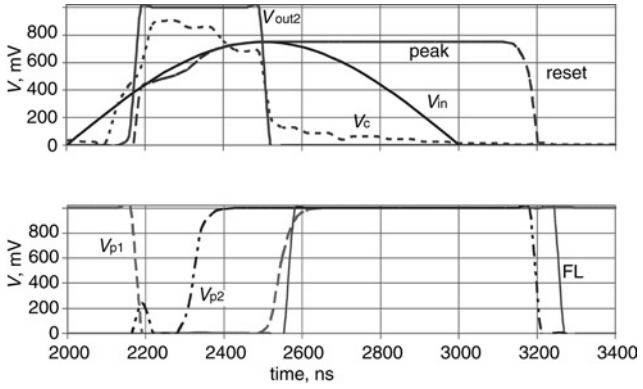

Fig. 3 *Operation of peak detector (top) and flag generation circuitry (bottom) for pulse signal amplitude of 0.75 V and 1 μs pulse width*

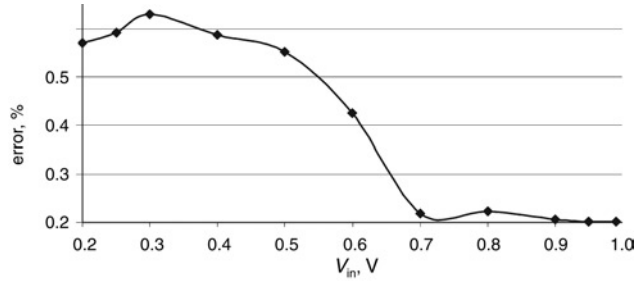

Fig. 4 *Peak detector accuracy (%) against input amplitude*

Conclusions: A high-precision peak detector for a medical imaging readout ASIC has been presented. The proposed circuit is based on a current-mode sampled latching mechanism and is very flexible in offering implementation trade-offs between power dissipation, achieved precision and expected input pulse widths. Adjustments of the clock frequency and the I_{level} reference current enable control of the input signal frequency in a wide range. For a power supply of $V_{DD} = 1$ V, the circuit uses an average energy of 20 pJ per one impulse and is 2.5 times better than the solution presented in [4], where energy per pixel is more than 50 pJ.

13 January 2007
Electronics Letters online no: 20070117
doi: 10.1049/el:20070117

R. Dlugosz (*ECE Department, University of Alberta, Edmonton, AB, Canada T6G 2V4 and University of Neuchâtel, Institute of Microtechnology, Rue A.-L. Breguet 2, CH-2000, Neuchâtel, Switzerland*)

E-mail: rdlugosz@ualberta.ca

K. Iniewski (*CMOS Emerging Technologies Inc., 2865 Stanley Pl., Coquitlam, BC, Canada V3B 7L7*)

References

1 Spieler, H.: 'Semiconductor detector systems' (Oxford University Press, 2005)
2 De Geronimo, G., O'Connor, P., and Grosholz, J.: 'A generation of CMOS readout ASIC's for CZT detectors', *IEEE Trans. Nucl. Sci.*, 2000, **47**, pp. 1857–1867
3 Anghinolfi, F., Dabrowski, W., Delagnes, E., Kaplon, J., Koetz, U., Jarron, P., Lugiez, F., Posch, C., Roe, S., and Weilhammer, P.: 'CTA-a rad-hard BiCMOS analogue readout ASIC for the ATLAS semiconductor tracker'. IEEE Nuclear Science Symp., Conf. Rec, November 1996, Vol. 1, pp. 46–50
4 Chen, C.M.H., Cook, W.R., Harrison, F.A., and Lin, J.Y.Y.: 'Characterization of a large-format, fine-pitch CdZnTe pixel detector for the HEFT balloon-borne experiment', *IEEE Trans. Nucl. Sci.*, 2004, **51**, (5), pp. 2472–2477
5 De Geronimo, G., Kandasamy, A., and O'Connor, P.: 'Analog peak detector and derandomizer for high-rate spectroscopy' (Part 1), *IEEE Trans. Nucl. Sci.*, 2002, **49**, (4), pp. 1769–1773
6 Cook, W.R., Burnham, J.A., and Harrison, F.A.: 'Low-noise custom VLSI for CdZnTe pixel detectors', *Proc. SPIE*, 1998, **3445**, pp. 347–354