Poznań University of Technology

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Design and optimization of finite impulse response electronic filters integrated in the CMOS technology

Ph. D. Dissertation

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to Jesus Christ
my God and Saviour

Contents

List of symbols and abbreviations

A — open loop gain of the operational amplifier
ASIC — application specific integrated circuit
CC — coefficient capacitor
C_{C} — number of combinations of clock phases in the multi-C structure
div — natural division without rest
DSP — digital signal processor
f_{clk} — frequency of the clock signal
f_{in} — frequency of the input signal
FIR — finite impulse response
I_{DD} — drain supply current
I_{SS} — source supply current
L_{CC} — number of coefficient capacitors
$L_{h\mathrm{CC}}$ — number of capacitors in the filter coefficient h_i in the multi-C structure
$L_{h\mathrm{CM}}$ — number of minimal capacitors with area S_{CM}
L_{OA} — number of operational amplifiers
L_{S} — number of switches
L_{UC} — number of unit capacitors
mod — rest obtained from the natural division
MOS — metal-oxide-semiconductor
OA — operational amplifier
N — order of the finite impulse response filter
P — number of clock phases
P_{CC} — chip area of the coefficient capacitors
P_{DEL} — chip area of the delay line
P_{OAW} — chip area of the output operational amplifier
P_{SP} — chip area of the switches and clock pathes in the summer circuit
R — order of the "even" and "odd" delay elements
RISC — reduced instruction set computer
round — rounding of a real number
S — switch
S_{C} — chip area of a single connection
S_{CC} — chip area of a single coefficient capacitor
S_{CM} — chip area of the minimal capacitor in the filter coefficient h_i
S_{CT} — chip area of capacitors in all filter coefficients
S_{OA} — chip area of a single operational amplifier
S_{S} — chip area of a single switch

S_{UC} — chip area of a single unit capacitor
$S(N)$ — total chip area
SC - switched capacitor
S&H — sample & hold delay element
SNR — signal-to-noise ratio
U_{off} — offset voltage
UC — unit capacitor
V_{ACT} — activation on/off voltage
V_{B} — bias voltage
V_{DD} — drain supply voltage
V_{SS} — source supply voltage
VLSI — very large scale of integration

Chapter 1

Introduction

1.1 Research area

Revolution in the monolithic integration of electronic filters began in the seventies with achievements in MOS VLSI (metal-oxide-semiconductor very large scale of integration) technology.

On the one hand, the ease of integrating perfect switches, precise capacitors (or more rigorously – precise capacitance ratios) and satisfactorily good operational amplifiers (OA's) led to an entirely new class of analog circuits, namely, to the switched-capacitor circuits (or SC circuits for short), i.e., circuits containing switches, capacitors, and active elements (e.g., OA's) [1].

On the other hand, however, digital single-chip integrated filters were developed concurrently to SC filters and the milestone on this way were general-purpose digital signal processors (DSP's) [4].

Construction of first SC filters was based on replacement of resistors present in classical active-RC filters by configurations of switches and capacitors. Direct approach to the design of SC filters is, however, also possible and in fact very promising. In this thesis the direct approach is considered and developed to the design and optimization of a very important class of filters, namely the FIR (finite impulse response) filters.

SC techniques have a lot of important advantages. The most important of them are: low power consumption for applications with low dynamic range, simple structure (low production costs) and a large degree of parallelism in the realization of certain signal processing tasks [1]. Thus, SC circuits can be preferable even for processing of signals at relatively high frequencies (in the range of MHz for modern sub-micron CMOS technology).

In SC techniques, the filter length is, in general, independent of the maximum frequency but is limited by the maximum chip area and by the minimum signal-to-noise ratio (SNR) [1, 2]. The chip area depends on the technology (among the currently used technologies are: 0.35 μm, 0.8 μm, and sometimes still 2 μm or 3 μm CMOS).

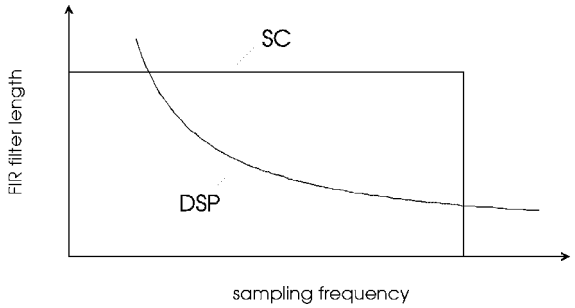


Figure 1.1: Performance limits for SC and DSP techniques [1]

It has to be stressed that around the seventies, digital systems started to replace analog solutions in almost all signal processing applications [6, 7, 31, 32]. One might even think that the era of classical frequency-domain signal processing, i.e., of high-precision analog filters, would have come to the limit, perhaps even to the end. This statement is, however, obviously not true. The need for constant miniaturization of electronic filters and the prolonged battery life (e.g., in portable units such as mobile phones) makes low-power and low-voltage design criteria more and more important for both analog and digital integrated circuits and in many situations favors analog (e.g., SC) solutions. Smaller dimensions and higher densities reduce the isolation barriers to a few volts and the power preventing chips from overheating to some milliwatts. For certain applications (in particular for the low-power and low-voltage case) switched-capacitor circuits have distinct advantages over their all-digital counterparts. The most important among them are:

- lower power consumption by about two orders of magnitude for applications in which a low dynamic range can be tolerated,
- simpler structure, resulting in lower design and production costs,
- larger degree of parallelism in the realization of certain signal processing algorithms.

From above properties it results that SC circuits, compared to digital realizations based on currently available DSP's [4, 49, 53], can be preferable for processing of signals at relatively high frequencies (i.e., in the range of several hundred kilohertz) as is illustrated in Fig. 1.1.

For a switched-capacitor realization, the filter length is limited by the maximum chip area and by the minimum signal-to-noise ratio (SNR) requirements. The upper limit for the sampling frequency, i.e., for the frequency range, is determined for SC filters by the bandwidth of OA's and by the maximum value of $\tau \approx RC$, where R is the on-resistance of the switches and C is the maximum effective capacity in the circuit, which, in turn, is governed by the used technology. Owing to a CMOS process, frequencies of several hundred kilohertz can be achieved using clock rates of up to several megahertz.

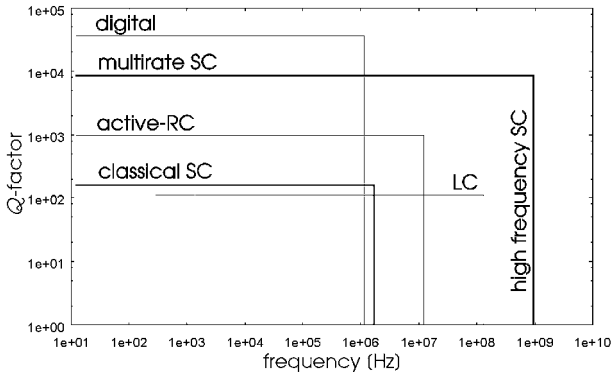


Figure 1.2: Transfer function Q-factor and frequency range limits for SC, digital, active-RC and LC filters [1]

For higher frequencies a faster process should be used, e.g., with a gallium arsenide (GaAs) technology.

For DSP realizations the maximum signal frequency depends on the operation cycle duration. For FIR filters of very small length, this maximum frequency limit is, as a rule, higher than that for an SC counterpart. Unfortunately, the required filter lengths are usually too large to be able to utilize this advantage. Thus, for most applications (those requiring large filter lengths) the resulting achievable sampling rate of a single DSP realization is relatively low. Accordingly, for typical sampling rates below, say 1 MHz, and filter lengths of the order of 50, the limits of realizability clearly favor SC implementations, as is confirmed in Fig. 1.1.

An important filter performance criterion is the attainable transfer function Q-factor, which is measure of the filter selectivity, i.e., the reverse of the relative passband width. The approximate performance capabilities, which can be achieved for the most important filter types are illustrated in 1.2.

The vertical axis shows the attainable Q-factor and the horizontal axis - the achievable operating frequency range. Typical SC filters are characterized by Q-factors limited to about 100 due to the limit on the maximum capacity ratio (the maximum capacitance is limited by the maximum realizable chip and the minimum capacitance by the technological tolerance and the requirements for the minimum SNR). Attainable Q-factor can, however, be extended to some thousands using multirate techniques. On the other hand, the frequency range limit of several hundreds of kilohertz can be extended to about 100 MHz by replacing CMOS technology by GaAs technology and also by the use of fast-settling OA's.

For comparison, classical LC filters can attain Q-factors of about 100 and the frequency range of the order of 100 MHz; but below say 1 kHz they become bulky and cumbersome. Active-RC filters can be designed for Q-factors up to about 1000 and for frequencies to around 10 MHz. Digital filters can achieve quite high Q-factors but they can operate up to only about 1 MHz with a single DSP realizations.

As we can see, particularly for low-power, low-voltage and/or low-dynamic range applications, as well as, for high Q values and high-frequency applications including multirate systems and filter banks, SC realizations can be clearly preferable to other analog approaches and to all-digital approaches. Moreover, SC circuits will dominate in implementation of the interface circuitry on the border between digital and analog systems. That is why considerations contained in this thesis are concentrated on SC realizations.

1.2 Aim and scientific thesis

Scientific aim of this Ph. D. dissertation is the development of the design and optimization methods for electronic switched-capacitor (SC) finite impulse response (FIR) filters for their integration in the contemporary CMOS technologies [1, 9, 20]. This is a specific but in fact the most important class of analog integrated FIR filters.

Scientific thesis can be formulated as follows: the proposed, designed, and optimized SC FIR filter structures, realized in contemporary sub-micron CMOS technologies, are suitable for high frequencies and dynamic ranges. Thus, their application in modern communication and multimedia systems is not only possible but also favorable in relation to the application of all-digital solutions.

To prove this thesis a representative illustrative example has been chosen, namely the channel filter for the GSM (global system for mobile telephony) system. Various versions of such a filter have been designed, integrated, realized, and measured.

The considered (existing and proposed new) SC FIR filter structures have been evaluated from the perspective of the efficiency of their integration and the perfection of their operation. The proposed evaluation process, used in this dissertation, is comprised of various criteria such as the chip area, clock system complexity, power consumption, and the output signal quality. Three following evaluation stages have been distinguished.

The first stage is a very quick, rough, and efficient theoretical comparison of SC FIR architectures, which uses only a general knowledge of the number of various elements. In this stage the design of the whole integrated circuit is not necessary, which is obviously a very important advantage of this approach. The most important advantage consists in the fact that the evaluation results obtainable using this method occurred to be very plausible.

For instance already at this stage it was possible to prove that filters with a relatively large spread of coefficients, typical for higher order selective filters, are not realizable as SC circuits, opposed to their all-digital counterparts. In a digital case large spread of coefficients is usually only a problem of secondary importance. This is, however, not the case for SC filters, because a very large chip area would be required to realize them. That is why an optimization method has been proposed, which consists in a division of an original, i.e., single, and usually quite long filter into a cascade of shorter sections. It has been shown that after the proposed optimization the spread of coefficients in

each of such sections is substantially lower. This considerably reduces the required chip area – typically even by many orders of magnitude.

Already at this stage it was also possible to evaluate many SC FIR filter families, among them a new family based on the so-called even-odd delay line structures [1]. Furthermore, introduction of the higher order even-odd delay line structures allows for improvement of many parameters.

The second evaluation stage is certainly the design and optimization of the whole integrated circuit in a prescribed technology and its verification by a large number of simulations. This is a necessary but very arduous stage.

The third and last stage is certainly the chip fabrication and then its measurement. Selected SC FIR filters have been fabricated and successfully verified.

The proposed three stage design and optimization process has proved to be very effective and efficient. Experiences gained at the first stage have been very useful at the second stage and finally resulted in successful chips with optimized parameters.

Chapter 2

General characteristic of switched capacitor circuits

2.1 Basics of the SC technique

In the seventies of the 20th century there began a revolution in the integration of electronic filters with important achievements in MOS VLSI technology. It became possible to integrate perfect switches, precise capacitors (with respect to capacitance ratios), and good operational amplifiers (OA's) [60, 61, 62]. This led to entirely new class of analog circuits - the switched-capacitor (SC) circuits [1, 9, 11]. The main idea of this kind of circuits lies in the possibility of replacing resistors with configurations of switches and capacitors. Combinations of switches and capacitors simulate resistors. The basic theoretical considerations presented in this Chapter are based on the book [1] written by the promoter of this thesis.

An illustrative circuit and the clock control with two clock phases ("e" and "o") is presented in Figure 2.1. T is the time period of the clock.

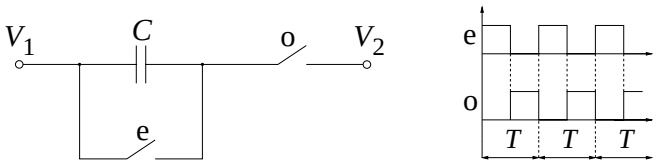


Figure 2.1: SC realization of a resistor and clock control

In the time period $\Delta t = T$ the charge, which flows trough the capacitor is given by equation (2.1). In practice, this charge can be interpreted as a Δq in the time period T.

$$q = U \cdot C = (V_1(t_n) - V_2(t_n)) \cdot C\,. \tag{2.1}$$

Current in the capacitor is given by equation (2.2)

$$i_{\mathrm{C}}(t_n) = \frac{\Delta q}{\Delta t} = \frac{U \cdot C}{T}\,. \tag{2.2}$$

If we replace capacitor and switches by the resistor with resistance R, current will be the same as in equation (2.3)

$$i_{\mathrm{R}}(t_n) = \frac{U}{R}\,. \tag{2.3}$$

Thus we can write

$$I_{\mathrm{C}} = I_{\mathrm{R}} \text{ for } R = \frac{T}{C}\,. \tag{2.4}$$

Above equations show that SC filters are the discrete-time circuits, with the analog representation of the voltage signal. Such circuits can be easily realized in different CMOS technologies, because they do not need resistors. This feature is important as CMOS technologies, which are relatively cheap, do not contain high-resistive layers, and as a result the integration of resistors is a difficult task. In the BiCMOS technologies the high-resistive layers are present, but these technologies are much more expensive than the CMOS.

2.2 Building blocks of the SC FIR filters

SC FIR filters contain only three basic elements, such as: switches (S's), unit (UC's) and coefficient (CC's) capacitors and operational amplifiers (OA's). These elements are parts of the basic building blocks such as the memory elements and summer circuits. Many different SC memory elements have been proposed in literature [3, 10, 21, 22, 23, 24, 25, 26, 27, 28, 29] . Summer circuits [2, 30] in SC technique join two different functions: multiplication and addition of the signal samples. Illustrative memory elements and summer circuits are shortly described below.

2.2.1 SC memory elements

Sample & hold delay element

This element (see Figure 2.2) stores the signal sample in the capacitor. The OA works in the follower configuration and the output of the OA is equal to the value of the signal sample. The sample can by read many times, what is an advantage of this kind of circuits. Signal sample is stored in the l phase and can be read in the any phase m. Output voltage as a function of the input voltage is given by equation (2.5)

$$u_{\mathrm{out}}(m) = \frac{1}{1+1/A}(u_{\mathrm{in}}(l) + u_{\mathrm{off}}) \approx u_{\mathrm{in}}(l) + u_{\mathrm{off}}\,. \tag{2.5}$$

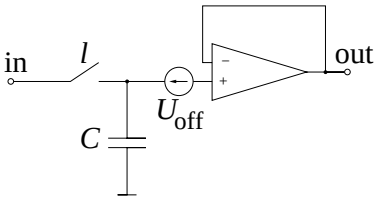


Figure 2.2: Sample & hold memory element

where A is an open loop gain of the OA, u_{off} is the OA offset voltage.

Nagaraj memory element

Figure 2.3 illustrates the delay element proposed by Nagaray [25]. This element is driven by a two phase clock, what is advantageous. Analysis of this circuit leads to equation (2.6)

$$(C_1 + \frac{C_1 + C_{s1} + C_s}{A}) \cdot u_{\text{out}}(nT) = \\ C_1 u_{\text{in}}((n-1)T) + \frac{C_s}{A} u_{\text{out}}((n-1)T) + (C_1 + C_{s1}) u_{\text{off}} \,. \tag{2.6}$$

Disadvantage of this memory element is the fact that the output voltage depends on the offset voltage of the OA. Assuming $A \to \infty$ and $U_{\text{off}} \to 0$ equation (2.6) reduces to equation (2.7)

$$u_{\text{out}}(nT) = u_{\text{in}}((n-1)T) \,. \tag{2.7}$$

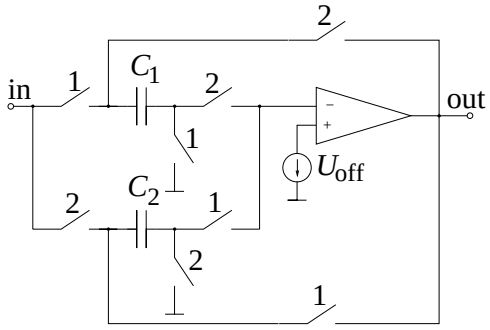


Figure 2.3: Nagaray memory element

Gilligham delay element

In Figure 2.4 two versions of the Gillingham delay element are presented. First block (a) is used at the beginning of the delay line and the second block (b) is used for all

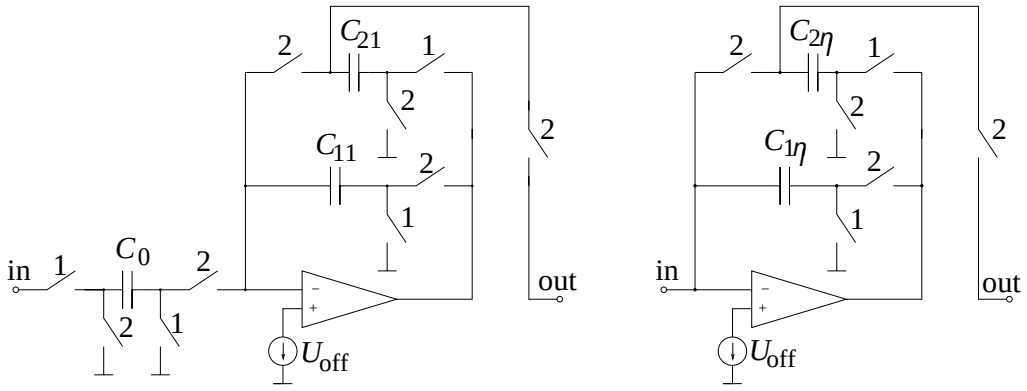


Figure 2.4: Gillingham delay elements: (a) used at the beginning of the delay line (b) used for all other delay elements

other delay elements in the delay line. The Gillingham delay element is driven by a two phase clock, which is advantageous. For these elements we can write the equations (2.8) and (2.9)

$$u_1\left((n+1)T\right) = \frac{C_0}{C_{11}} u_{\text{in}}(nT) + u_{\text{off1}}\,, \tag{2.8}$$

and

$$u_1\left((n+2)T\right) = \frac{C_{11}}{C_{21}} u_1\left((n+1)T\right) + u_{\text{off1}} - u_{\text{off2}}\,. \tag{2.9}$$

Notice that for the block (b) we have

$$u_{\text{in}\eta}(nT) = u_{\text{off}\eta}\,. \tag{2.10}$$

Thus we obtain

$$u_\eta((n+2\eta-1)T) = \frac{C_{2(\eta-1)}}{C_{1\eta}} u_{\eta-1}([n+2(\eta-1)]T) - u_{\text{off}(\eta-1)} + u_{\text{off}\eta}\,, \tag{2.11}$$

and finally

$$u_\eta((n+2\eta)T) = \frac{C_{1\eta}}{C_{2\eta}} u_\eta((n+2\eta-1)T) - u_{\text{off}\eta} + u_{\text{off}(\eta+1)}\,. \tag{2.12}$$

Assuming, that all capacitors have the same capacities, we can write

$$u_\eta\left((n+2\eta-1)T\right) = u_{\text{in}}(nT) + u_{\text{off1}}\,, \tag{2.13}$$

and

$$u_\eta((n+2\eta)T) = u_{\text{in}}(nT) + u_{\text{off}1} + u_{\text{off}\eta} - u_{\text{off}(\eta+1)}\,. \tag{2.14}$$

These equations show, that this element is sensitive to the offset voltage of a practically single OA, however, this is due to sensitivity to capacitor mismatch.

Even and odd delay elements

Dąbrowski, Menzi, and Moschytz proposed in 1989 the delay elements, which are offset voltage compensated and are insensitive to the capacitor mismatch. There exist two basic versions of them: even and odd delay element, which should be connected alternately in the delay line. Analysis of these elements is presented in Section 3.6.

2.2.2 SC summer circuits

Lee-Martin summer

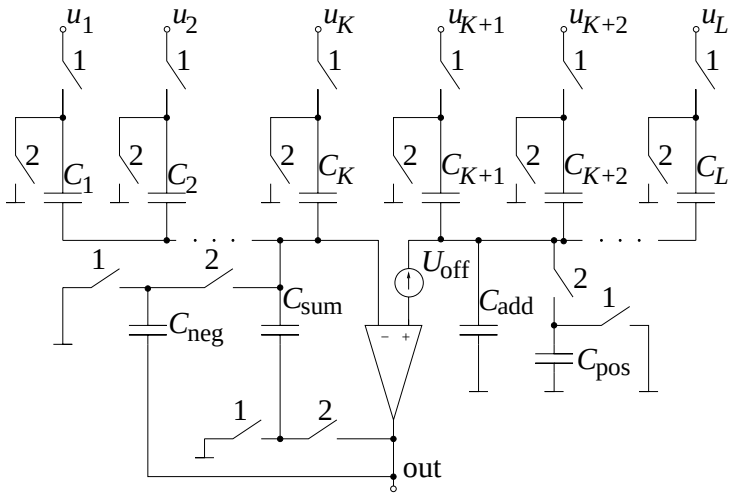


Figure 2.5: Lee-Martin summer

The output voltage as a function of the input voltages is given by equation (2.15)

$$u_{\text{out}}(nT) = -\sum_{i=1}^{K} \frac{C_i}{C_{\text{sum}}} u_i(nT) + \sum_{i=K+1}^{L} \frac{C_i}{C_{\text{sum}}} u_i(nT)\,. \tag{2.15}$$

under convenient assumption that $C_{\text{sum}} + \sum_{i=1}^{K} C_i = C_{\text{add}} + \sum_{i=K+1}^{L} C_i$. This circuit is offset voltage compensated in the first clock phase.

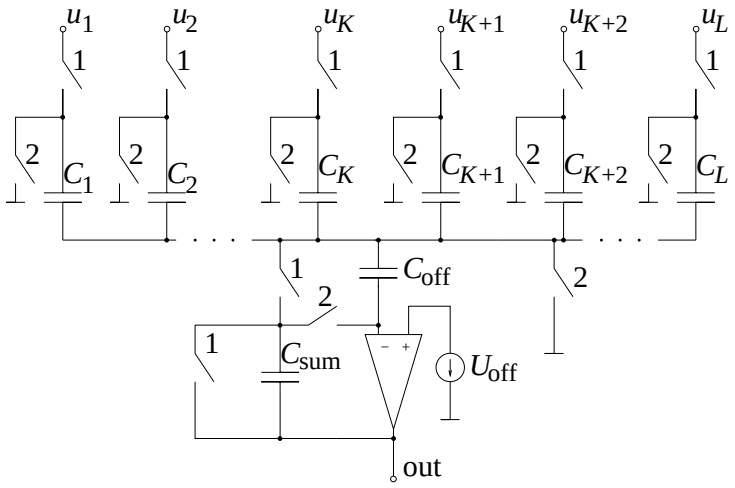


Figure 2.6: Recharge summer

The output voltage as a function of the input voltages is given by equation (2.16)

$$u_{\text{out}}(nT) = -\sum_{i=1}^{K} \frac{C_i}{C_{\text{sum}}} u_i((n-1)T) + \sum_{i=K+1}^{L} \frac{C_i}{C_{\text{sum}}} u_i((n-1)T)\,. \tag{2.16}$$

2.3 Theoretical SC FIR filter architectures

The family of the SC FIR filters contains different architectures, presented briefly in this subsection. These structures posses both advantages and disadvantages. In practice it is necessary to seek the compromise between these features for each particular application.

There exist basic SC FIR filter structures and composite structures, which are compositions of the basic structures.

2.3.1 Basic SC FIR filter structures

- **Delay line structures:** These architectures are either a tapped delay line structure or as a reversed delay line structure. Both of them can be realized in parallel ("data read" and "data write" operations are performed in the same phases in all delay elements) or serially (i.e., one after the other, thus composing a single filter operation cycle). In the first case, a great number of OA's, and a small number of clock phases are necessary. Structures of this kind can be based either on even-odd delay elements [1, 3] (structure No. 1, see Figure 2.7) or on Gillingham delay element (structures No. 2 and 3, see Figures 2.8 and 2.9). Advantages and

disadvantages of each of these structures result, in particular, from properties of the even-odd (see Section 3.6) and the Gillingham delay elements. Among advantages of the even-odd delay elements are: compensation of the offset-voltage and insensitivity to the capacitor mismatch. The last property results from the fact that U_{out} in the even and odd delay elements are independent of the values of capacitors. Structure No. 1 is driven by a four phase clock but with only two clock phases per sample. On the other hand, the Gillingham element requires only a two phase clock. The disadvantage of structures No. 2 and No. 3 is their sensitivity to capacitor mismatch and to offset-voltage. Nevertheless, the offset errors do not accumulate along the delay line, what is obviously an important advantage.

In the case of serial realizations, a single OA suffices but a complex multiphase clock is required (delay line structures No. 4 and 5, see Figures 2.10 and 2.11). Structure No. 5 realizes a reversed delay line.

The main disadvantage of all delay line structures is their sensitivity to overwrite errors accumulated along the line during the "data read" and "data write" operations.

- **Rotator FIR structure:** This structure comprises the so-called rotator switch that connects signal samples with capacitors of the summer circuit (see Figures 2.13, 2.14 and 2.15). The signal samples are stored in sample-and-hold delay elements. Structures of this kind are characterized by large numbers of OA's and many switching phases, but the clock system is a simple structure and particular switches are driven by only one clock phase. In these structures the upper frequency range does not depend on the filter order N, because only two clock phases occur during processing of one of the signal samples.

- **Parallel or multi-C FIR structure:** In this structure, signal samples are stored in individual capacitors. The advantages are: no cumulative errors (in opposition to the delay line structures) and a single active element only (see Figure 2.12). The disadvantages are: a great number of switching phases: $2(N+1)$, where N is the filter order, and a very large number of capacitors, i.e., about $(N+1)^2$. In this structure numerous switches are driven by more than one clock phase and this fact creates an additional problem, which concerns the separation of the clock phases.

2.3.2 Composite SC FIR filter structures

The disadvantages of particular basic structures become a problem when the filter order N is high. In such cases it is necessary to look for new solutions, which minimize disadvantages of basic structures. The problem can be solved to a certain degree by introducing a family of composite structures, i.e., those, which are composed of at least two basic structures. Composite structures allow realizing compromise solutions, in which disadvantages are reduced to substructures and in result are masked

by advantages of other substructures. However, composite structures are usually more complicated and thus more difficult in the CMOS realization.

Derivation of different composite SC FIR filter structures is based on the so-called "morphological approach" [17]. In this method we look for all realizable composite SC FIR filter structures. The morphological approach adapted to the design of composite SC FIR filters consists of the following five steps:

1. **Problem formulation:** We are going to realize composite SC FIR filter configurations using the basic SC FIR filter structures. Then we shall qualify them according to the following criteria: number of circuit elements, chip area, operation speed, network performance, clock complexity, etc.

2. **Characterization of fundamental elements:** The following four basic SC FIR structures serve as the fundamental elements for the so-called "morphological box": multi-op-amp delay line FIR structure, multiphase delay line FIR structure, parallel (multi-C) FIR structure, rotator FIR structure.

3. **Derivation of a morphological box:** In the case under discussion this is a multi-dimensional box with four basic structures (those listed above) placed along each dimension. The possible solutions correspond to different positions in the box. Theoretically we could consider composite structures containing an arbitrary number of stages realized with basic structures but practically we shall limit ourselves to two or at most three of them.

4. **Evaluation of solutions contained in the morphological box:** Many of the theoretically possible solutions are not realizable or unreasonable in practice. Thus we eliminate them using the following rules:

   - In order to reduce the number of OA's, the parallel (multi-C) FIR structure should be applied as the last link of a composite filter structure or followed by a delay line with recharge branches and recharge summer circuits. Signal samples (charges on capacitors) can be read only once.
   - A particular basic structure can (in practice) occur only once in a composite structure. Two consecutive identical basic structures can be combined into one. Configurations composed of more than two basic structures are of little practical concern.
   - Structures equivalent to a tapped delay line are suitable for the first link, while structures realizing the reversed delay line are well fitted for the last link.

   Taking the above conditions into account, we obtain 8 reasonable composite FIR SC configurations, which are presented in the next subsection.

5. **Evaluation of the solutions:** A selection of superior solutions among the FIR SC structures obtained in step 4 can be based on the evaluation of their feasibility as integrated circuits and on their performance in applications.

2.3.3 Diagrams of the basic and composite SC FIR filter structures

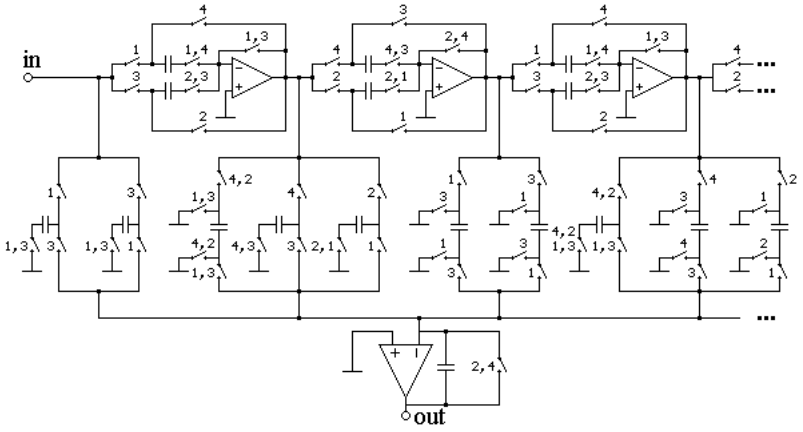


Figure 2.7: Delay line structure No. 1

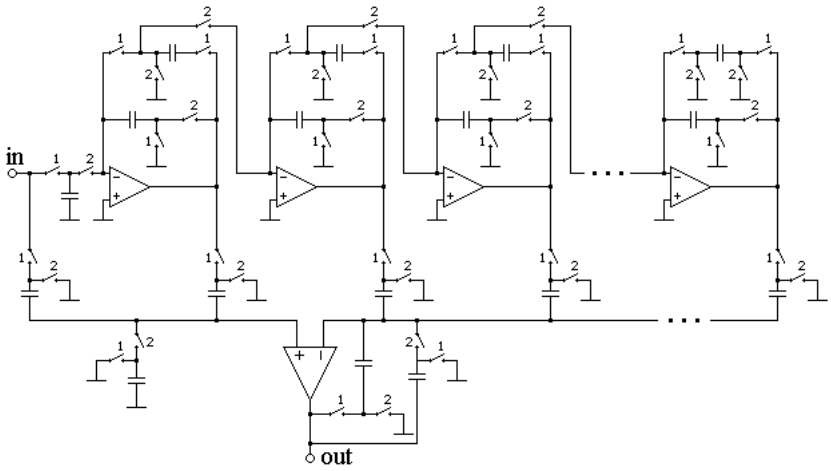


Figure 2.8: Delay line structure No. 2

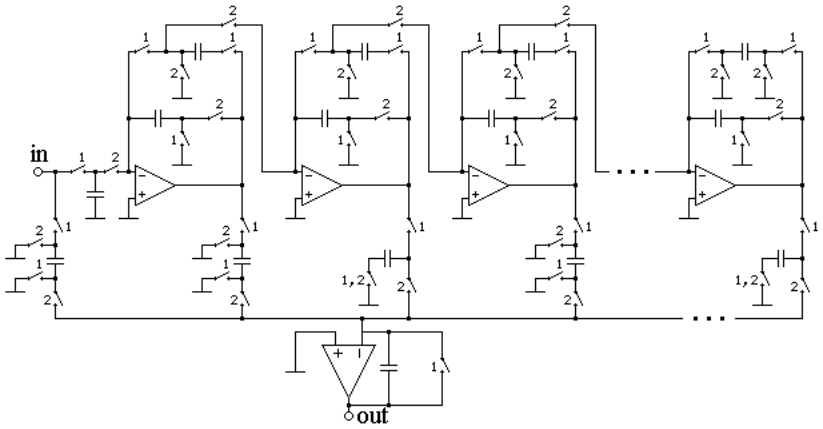


Figure 2.9: Delay line structure No. 3

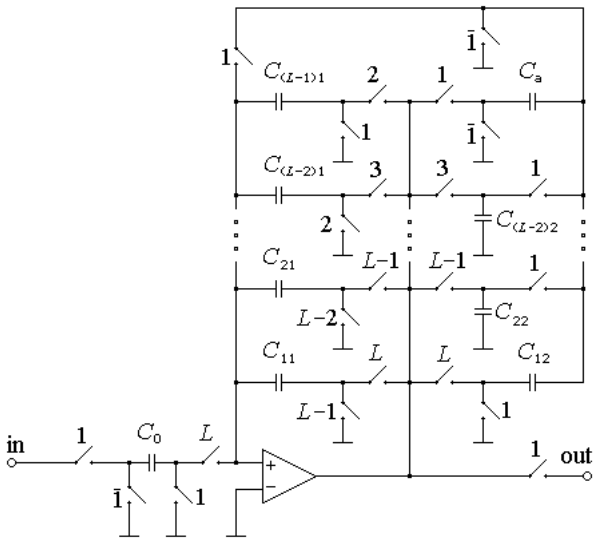


Figure 2.10: Delay line structure No. 4

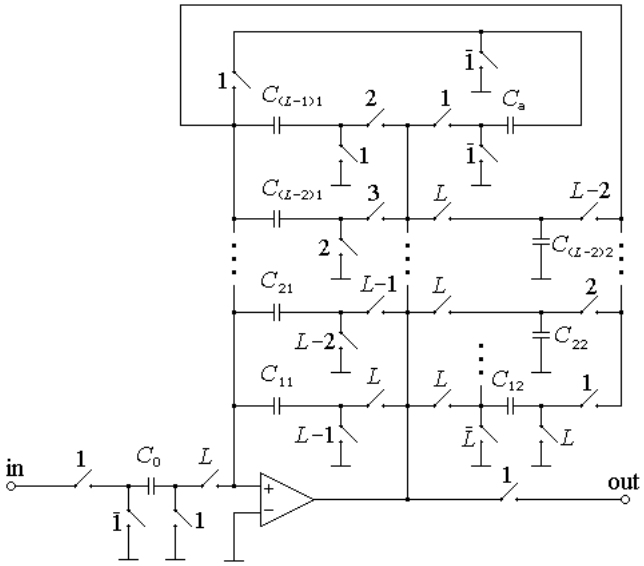


Figure 2.11: Delay line structure No. 5

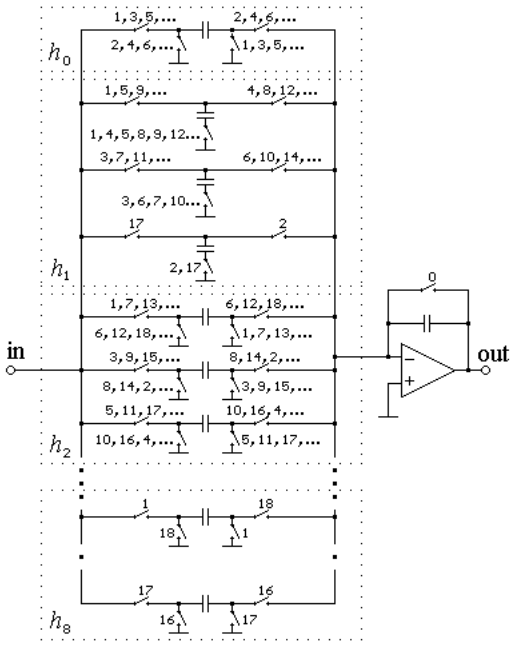


Figure 2.12: Multi-C structure for $N = 8$

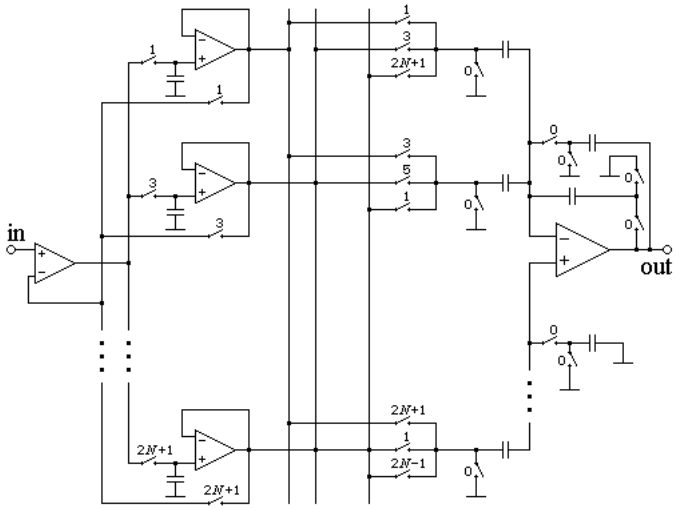


Figure 2.13: Rotator structure No. 1

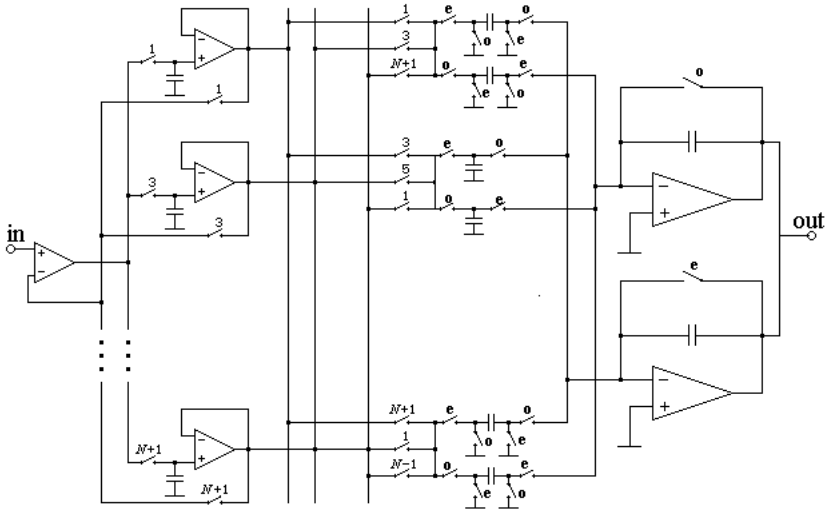


Figure 2.14: Rotator structure No. 2

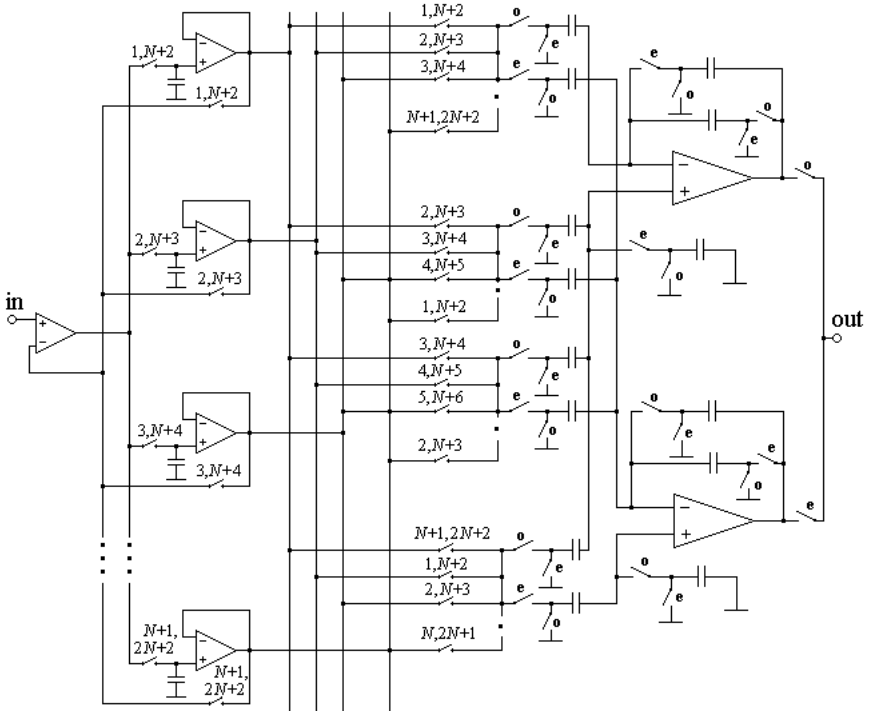


Figure 2.15: Rotator structure No. 3

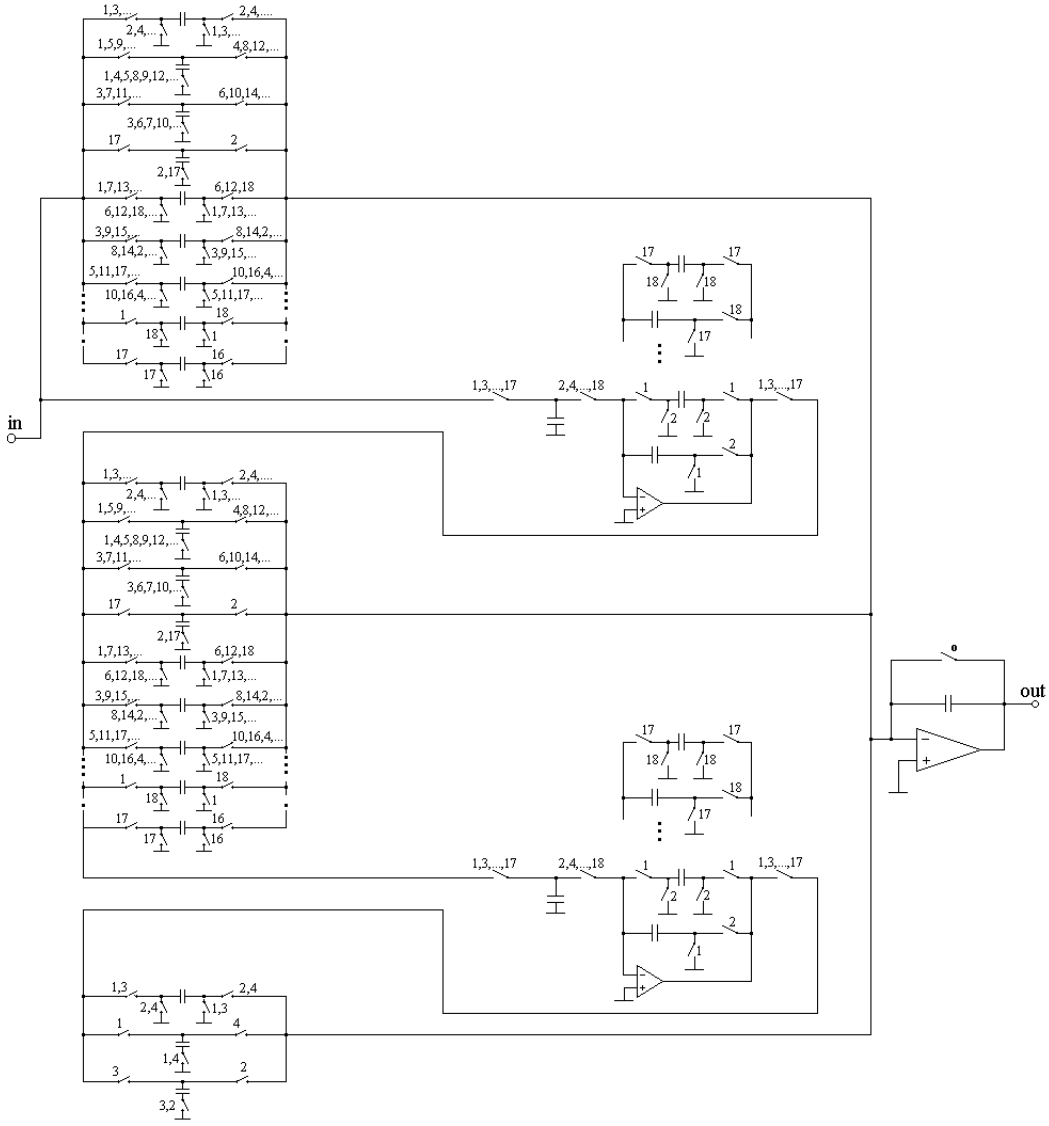


Figure 2.16: Delay line - multi-C structure

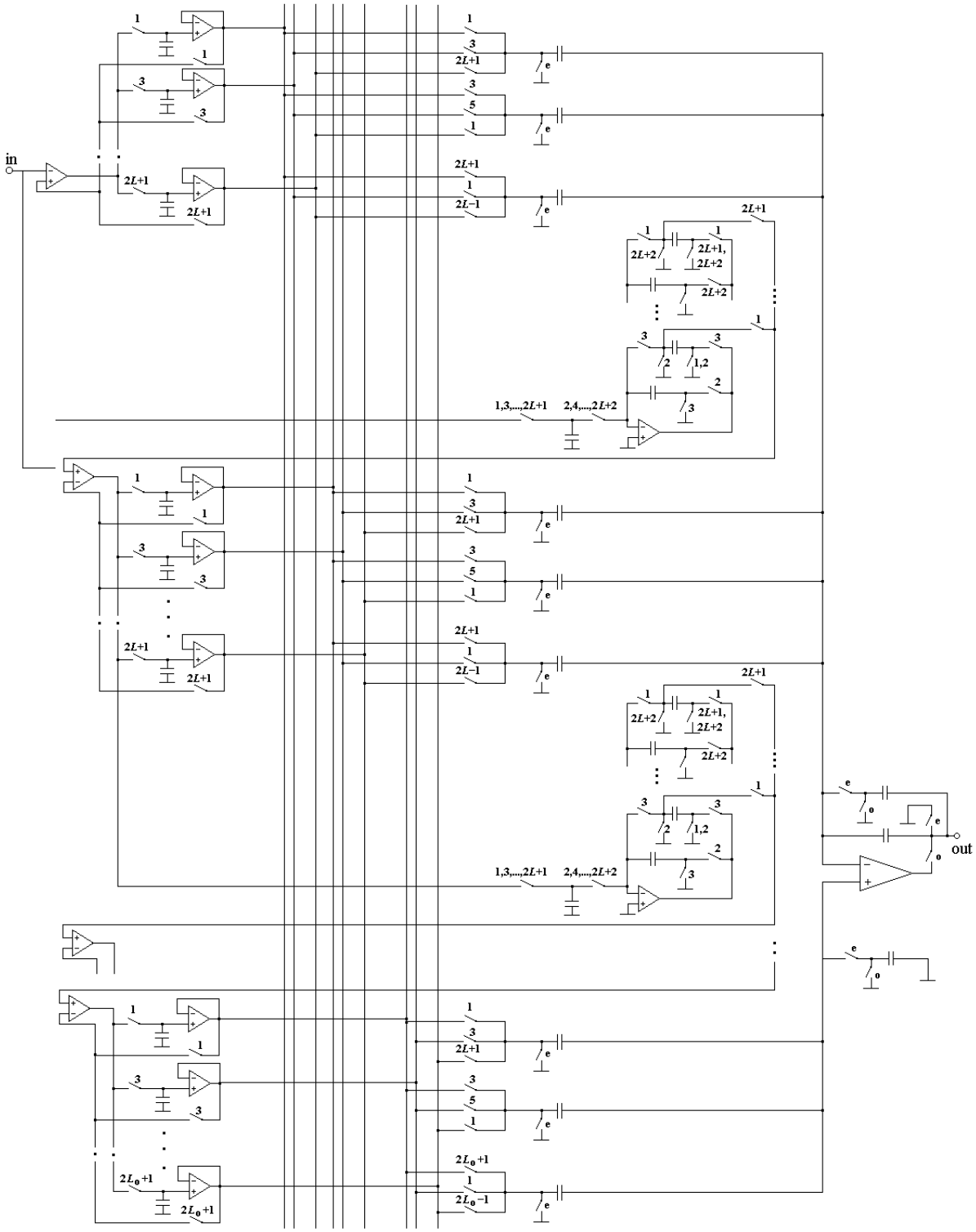


Figure 2.17: Delay line - rotator structure

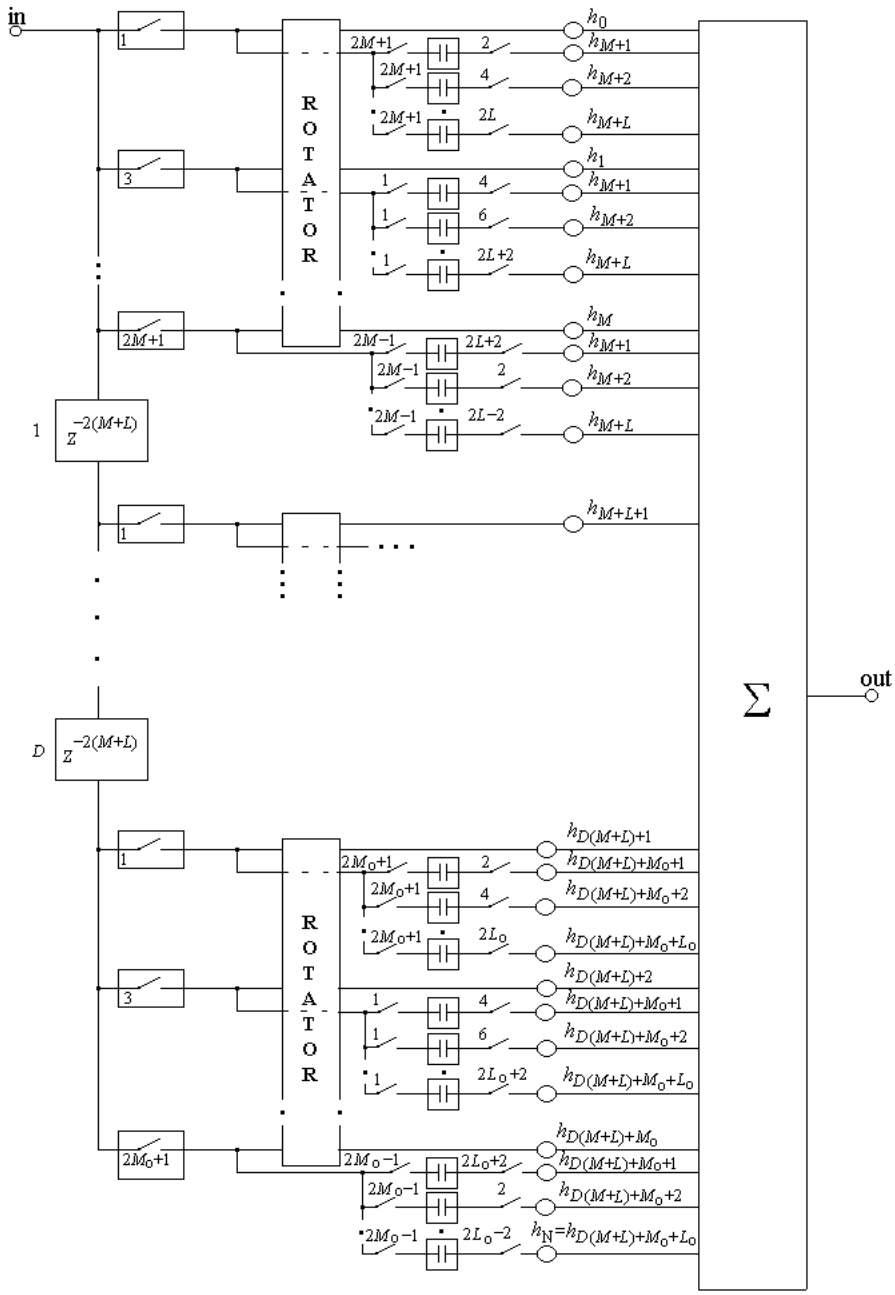


Figure 2.18: Delay line - rotator - multi-C structure

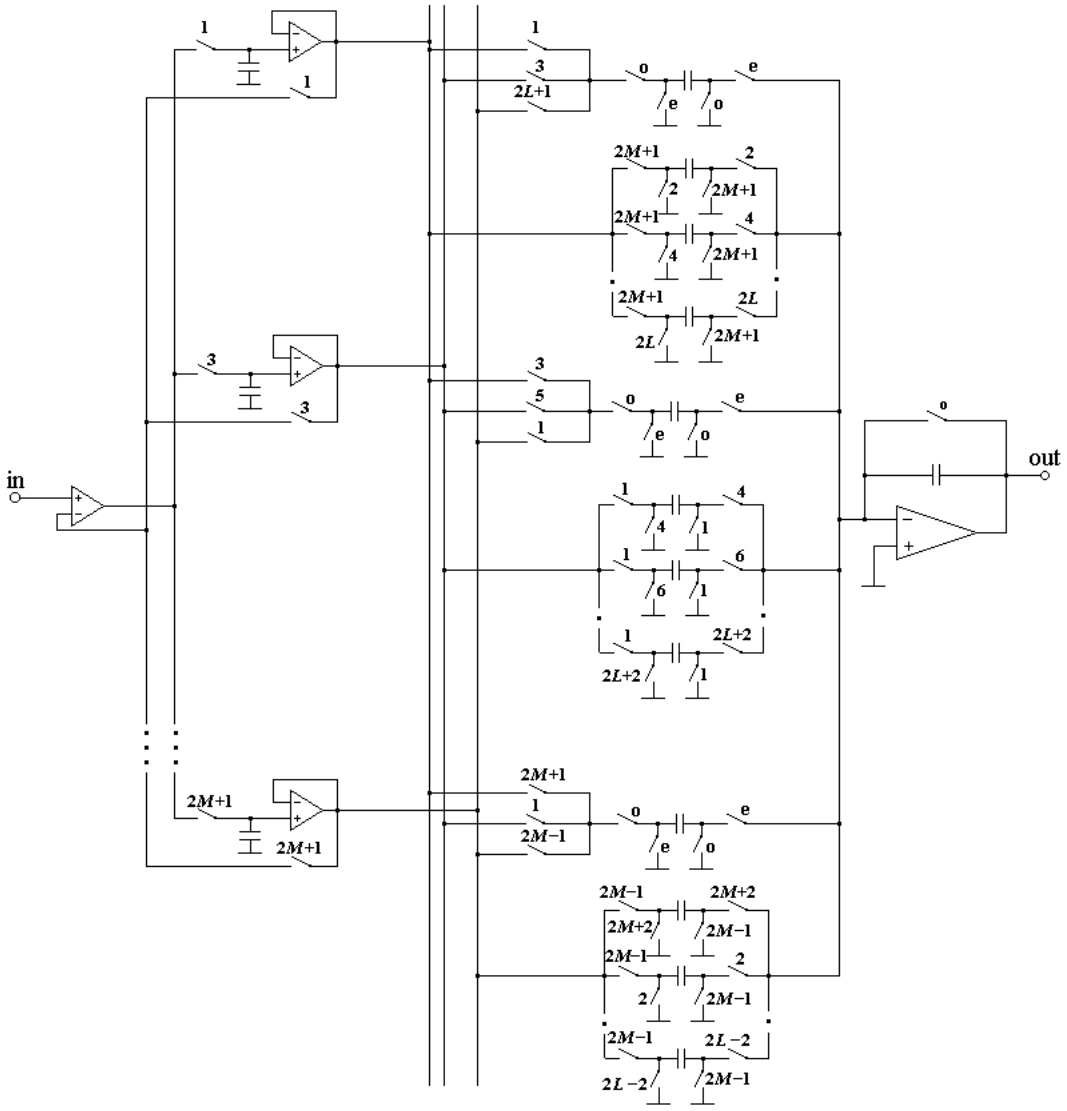


Figure 2.19: Rotator - multi-C structure

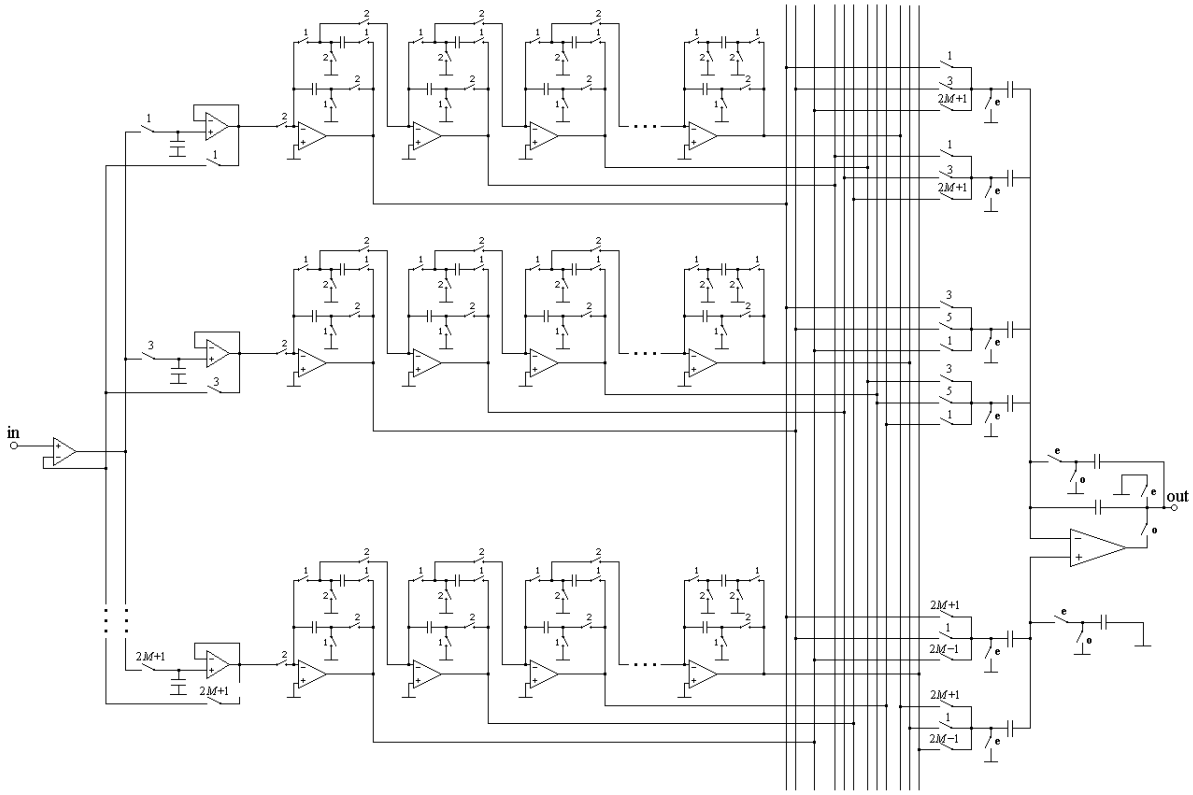


Figure 2.20: Rotator - delay line structure

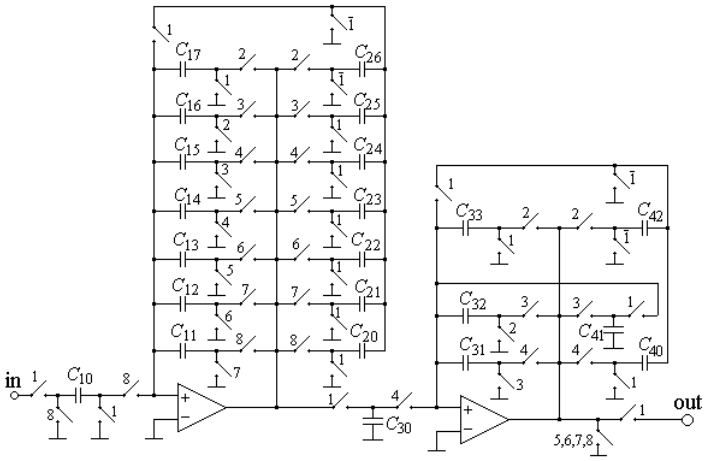


Figure 2.21: Fischer structure

Chapter 3

Comparison and evaluation of the SC FIR filter structures

In this Chapter the methods for comparing and evaluating the SC FIR filters are presented. One of the most important parameters is the chip area of the integrated circuit. This parameter exerts a great influence on the total cost of the integrated circuit.

The evaluation of the chip area on the basis of some theoretical assumptions presented in the next Subsection [33, 36], is a very simple and efficient method as it does not require the whole design process. It is, however, only a rough evaluation, although in most cases it offers plausible results.

The weakest assumption of the simplified approach are constant values of particular filter elements resulting in reservation of the constant chip areas for them. In reality the filter element values strongly depend on the filter frequency response. Thus estimation of the plausible substitute (averaged) element values is a very important task for this evaluation method.

In order to improve the exactness of the results of the simplified approach the author modified and improved it by taking actual element values into account [34, 48]. Using this new approach it was possible to show that for many practical filter frequency responses the required chip area is unrealistic large, if they are to be realized directly (like digital filters). In order to overcome this severe problem the author suggested a method for optimization (minimization) of the chip area. It is based on the following principle: a single high order (i.e. long) filter should be split into some shorter sections connected in a cascade.

The chip area evaluation method and the method for the minimization of the chip area are presented in the third Subsection of this Chapter. This method was used to compute optimum values of coefficients for filters realized as integrated circuits. They are presented in the fourth Chapter of this dissertation.

In the third Subsection of this Chapter we present a problem of realization of clock systems for SC FIR filters [38, 43, 49]. Particular SC FIR filter structures are driven

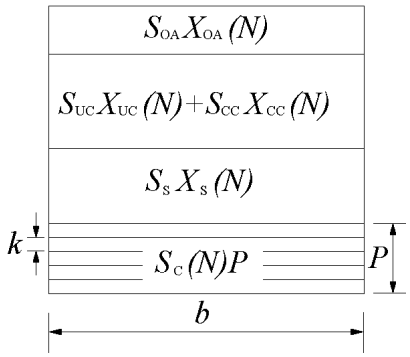


Figure 3.1: Theoretical organization of the chip area

by clock systems with different degrees of complexity. The clock systems effect many other parameters of the integrated circuit also the chip area. In this Subsection we also propose and compare different solutions for the clock systems.

In the next two Sections we compare SC FIR filters from the perspective of the power consumption and the quality of the signal processing.

Comparison of filters on the basis of all these different criteria led the author to postulating a new family of the even-odd delay line structures [46]. The even-odd delay line structures introduced earlier [1, 3] are in this thesis called the first order structures. The author postulates a family of higher order even-odd delay elements and consequently — higher order delay line structures. The resulting filters are presented and evaluated in the last Subsection of this Chapter.

3.1 Evaluation of the chip area on the basis of theoretical assumptions

3.1.1 Chip area estimation

To estimate the required chip area for a particular FIR structure, it is necessary to determine the number of the elements as a function of the filter order N [33, 36]. Then we consider the equation (3.1)

$$S(N) = S_{\mathrm{OA}}L_{\mathrm{OA}}(N) + S_{\mathrm{UC}}L_{\mathrm{UC}}(N) + S_{\mathrm{CC}}L_{\mathrm{CC}}(N) + S_{\mathrm{S}}L_{\mathrm{S}}(N) + S_{\mathrm{C}}(N)P\,, \qquad (3.1)$$

where:
$S(N)$ - the entire chip area, N - filter order, S_{C} - area of a single connection,
P - number of clock phases, S_{OA} - area of a single OA, $L_{\mathrm{OA}}(N)$ - number of OA's,
S_{UC} - area of a single unit capacitor (UC), $L_{\mathrm{UC}}(N)$ - number of UC's,

S_{CC} - area of a single coefficient capacitor (CC), $L_{CC}(N)$ - number of CC's,
S_S - area of a single switch (S), $L_S(N)$ - number of S's.

Assuming that the chip shape is approximately square (see Fig. 3.1), we can write

$$S_C = k\sqrt{S_{OA}L_{OA} + S_{UC}L_{UC} + S_{CC}L_{CC} + S_S L_S} = kb\,. \tag{3.2}$$

Coefficient S_C results from the necessity of assigning some part of the chip area for connections. This area depends linearly on the number of clock phases P. Coefficient k depends on the technology used, b is the length of the chip equal to the square root of the area of all filter elements. Coefficients S_{OA}, S_{UC}, S_{CC}, S_S depend also on the technology. We use their estimated values. The values for parameters L_{OA}, L_{UC}, L_{CC}, L_S, i.e., numbers of particular elements, are computed in the next Subsection individually for all considered structures.

3.1.2 Number of elements as a function of the filter order N

Equations given in tables below comprise the following denotations:

- div — the natural division without rest,
- mod — rest obtained from the natural division,
- round — rounding of a real number, in the used interpretation, e.g., round(2.50) = 2 but round(2.51) = 3 (for the purpose used in this Subsection rounding of numbers with more than two fractional digits is not necessary).

Table 3.1: Number of elements used in the delay line structure No. 1

	Delay line	Summer	Total
L_{OA}	$N-(N+1)$ div 3	1	$N+1-$ $(N+1)$ div 3
L_S	$7N-$ $7[(N+1)$ div $3]$	$6N+7-$ $3[(N+2)$ div $3]$	$13N+7-$ $7[(N+1)$ div $3]-$ $3[(N+2)$ div $3]$
L_{UC}	$2[N-(N+1)$ div $3]$	0	$2[N-(N+1)$ div $3]$
L_{CC}	0	$2+2N+1-$ $[(N+2)$ div $3]$	$3+2N-$ $[(N+2)$ div $3]$
P	4	4	4

Table 3.2: Number of elements used in the delay line structure No. 2 and 3

	Delay line No. 2			Delay line No. 3		
	Delay line	Summer	Total	Delay line	Summer	Total
L_{OA}	N	1	$N+1$	N	1	$N+1$
L_{S}	$6N+1$	$2N+8$	$8N+9$	$6N+1$	$3N+7$	$9N+8$
L_{UC}	$2N+1$	0	$2N+1$	$2N+1$	1	$2N+2$
L_{CC}	0	$N+4$	$N+4$	0	$N+2$	$N+2$
P	2	2	2	2	2	2

Table 3.3: Number of elements used in the delay line structure No. 4 and 5

	Delay line No. 4	Delay line No. 5
	Total	Total
L_{OA}	1	1
L_{S}	$4N+11$	$5N+11$
L_{UC}	$N+2$	$N+2$
L_{CC}	N+1	N+1
P	$2(N+1)$	$2(N+1)$

Table 3.4: Number of elements used in the delay line - multi-C structure

	Delay line	Multi-C - Summer	Total
L_{OA}	D	1	$D+1$
L_{S}	$D[3+6(L+1)]$	$3DC+3C_0+1$	$D(6L+9)+3DC+3C_0+1$
L_{UC}	$D[1+2(L+1)]$	0	$D(2L+3)$
L_{CC}	0	$DC+C_0+1$	$DC+C_0+1$
P	$2(L+1)$	$2(L+1)$	$2(L+1)$

where:
N - filter order, L - order of a previous multi-C section, L_0 - order of the last multi-C section, D - number of delay elements, and $D = (N+1)$ div $(L+1) - B$.
If $(N+1)$ mod $(L+1) = 0$ then $B = 1$ else $B = 0$; $L_0 = (N+1) - D(L+1)$. Number of capacitors in previous sections is equal to $C = [\frac{(L+2)(L+1)}{2} + \sum_{i=1}^{L}(L+1) \bmod (i+1)]$ and number of capacitors in the last section to $C_0 = [\frac{(L_0+2)(L_0+1)}{2} + \sum_{i=1}^{L_0}(L_0+1) \bmod (i+1)]$.

Table 3.5: Number of elements used in the delay line - rotator structure

	S&h	Delay line	Rotator	Summer	Total
L_{OA}	$1+N+1$	D	0	1	$N+D+3$
L_{S}	$2(N+1)$	$2D+$ $7D(L+1)$	$D(L+1)^2+$ $(L+1)^2$	$N+$ $1+6$	$3(N+1)+2D+$ $D(L+1)(L+8)+$ $(L_0+1)^2$
L_{UC}	$N+1$	$D+$ $2D(L+1)$	0	0	$N+1+$ $D(2L+3)$
L_{CC}	0	0	0	$N+$ $1+3$	$N+4$
P	$2(L+1)$	$2(L+1)$	$2(L+1)$	2	$2(L+1)$

where:
N - filter order, L - rotator order, L_0 - order of the last section, D - number of delay elements and $D=(N+1)$ div $(L+1)-B$. If $(N+1)$ mod $(L+1)=0$ then $B=1$ else $B=0$; $L_0=(N+1)-D(L+1)$.

Table 3.6: Number of elements used in the multi-C structure

	Multi-C	Summer	Total
L_{OA}	0	1	1
L_{S}	$3\frac{(N+2)(N+1)}{2}+$ $3\sum_{i=1}^{N}(N+1) \bmod (i+1)$	1	$3\frac{(N+2)(N+1)}{2}+$ $3\sum_{i+1}^{N}(N+1) \bmod (i+1)+1$
L_{UC}	0	0	0
L_{CC}	$\frac{(N+2)(N+1)}{2}+$ $\sum_{i=1}^{N}(N+1) \bmod (i+1)$	1	$\frac{(N+2)(N+1)}{2}+$ $\sum_{i+1}^{N}(N+1) \bmod (i+1)+1$
P	2		$2(N+1)$

Table 3.7: Number of elements used in the rotator structure No. 1

	Sample & hold	Rotator	Summer	Total
L_{OA}	$1+N+1$	0	1	$N+3$
L_{S}	$2(N+1)$	$(N+1)^2$	$N+1+6$	$(N+1)(N+4)+6$
L_{UC}	$N+1$	0	0	$N+1$
L_{CC}	0	0	$N+1+3$	$N+4$
P	$2(N+1)$	$2(N+1)$	2	$2(N+2)$

Table 3.8: Number of elements used in the rotator structure No. 2

	Sample & hold		Rotator	Summer	Total	
L_{OA}	$1+(N+1)$		0	2	$N+4$	
L_{S}	$2(N+1)$		$(N+1)^2$	$6(N+1)+4$	$(N+1)(N+9)+4$	
L_{UC}	$N+1$		0	0	$N+1$	
L_{CC}	0		0	$2(N+1)+2$	$2(N+1)+2$	
P	N_{odd} $N+1$	N_{even} $2(N+1)$			N_{odd} $N+1$	N_{even} $2(N+1)$

Table 3.9: Number of elements used in the rotator structure No. 3

	Sample & hold		Rotator	Summer	Total	
L_{OA}	$1+(N+1)$		0	2	$N+4$	
L_{S}	$2(N+1)$		$(N+1)^2$	$4(N+1)+14$	$(N+1)(N+7)+14$	
L_{UC}	$N+1$		0	0	$N+1$	
L_{CC}	0		0	$2(N+1)+6$	$2(N+1)+6$	
P	N_{odd} $N+1$	N_{even} $2(N+1)$			N_{odd} $N+1$	N_{even} $2(N+1)$

Table 3.10: Number of elements used in the delay line - rotator - multi-C structure

	Delay line	S&H	Rotator	Multi-C	Total
L_{OA}	D	$D(M+2)+$ (M_0+2)	0	1	$D(M+3)+$ (M_0+2)
L_{S}	$9D+$ $7DF$	$2[D(M+1)+$ $(M_0+1)]$	$D(M+1)^2+$ $(M_0+1)^2$	$1+$ $3[(1+L)\cdot$ $(M+1)D+$ $(M_0+1)\cdot$ $(1+L_0)]$	$D(M+1)\cdot$ $(M+3L+6)+$ $(M_0+1)\cdot$ $(M_0+3L_0+6)+$ $D(7F+3)+1$
L_{UC}	$3D+$ $2DF$	$D(M+1)+$ (M_0+1)	0	0	$D(4+2F+M)+$ M_0+1
L_{CC}	0	0	0	$1+$ $D(M+1)\cdot$ $(1+L)+$ $(M_0+1)\cdot$ $(1+L_0)$	$D(M+1)\cdot$ $(1+L)+$ $(M_0+1)\cdot$ $(1+L_0)+1$
P					$2(M+1)$

where:
M - rotator order; L - number of capacitors in a single multi-C section; F - order of previous sections of the rotator - multi-C type; M_0 - the last rotator order; L_0 - number of capacitors in the last multi-C section; F_0 - the last section rotator - multi-C order; D - number of delay elements; N - filter order; and $D = (N+1)$ div $(F+1) - B$; If $(N+1)$ mod $(F+1) = 0$ then $B = 1$ else $B = 0$; $F_0 = (N+1) - D(F+1)$; $M_{\min} =$ round $(F/2+0.01)$; $M_{0\min} =$ round $(F_0/2+0.01)$; $L = F-M$; $L_0 = F_0-M_0$.

Table 3.11: Number of elements used in the rotator - delay line structure

	S&H	Delay line	Rotator	Summer	Total
L_{OA}	$1+(M+1)$	$(M+1)L$	0	1	$(M+1)(L+1)+2$
L_{S}	$2(M+1)$	$(M+1)(1+6L)$	$(M+L+1)\cdot$ $(M+1)$	$M+L+$ $1+6$	$L+6+$ $(M+1)(7L+M+5)$
L_{UC}	$M+1$	$2L(M+1)$	0	0	$(M+1)(2L+1)$
L_{CC}	0	0	0	$M+L+$ $1+3$	$M+L+4$
P	$2(M+1)$	2	$2(M+1)$	2	$2(M+1)$

where:
M - rotator order, L - order of a single delay line, $N = M + L$.

Table 3.12: Number of elements used in the rotator - multi-C structure

	S&H	Rotator	MultiC	Summer	Total
L_{OA}	$1+M+1$	0	0	1	$M+3$
L_{S}	$2(M+1)$	$(M+1)^2$	$3L(M+1)$	$1+$ $3(M+1)$	$1+$ $(M+1)(M+3L+6)$
L_{UC}	$M+1$	0	0	0	$M+1$
L_{CC}	0	0	$L(M+1)$	$1+$ $(M+1)$	$(M+1)(L+1)+1$
P	$2(M+1)$	$2(M+1)$	$2L$	2	$2(M+1)$

where:
N - filter order, M - rotator order, L - number of capacitors in a single multi-C section and $M_{\min} =$ round $(N/2+0.01)$, $L = N - M$.

Table 3.13: Number of elements used in the Fischer structure

	previous sections	last section	Total
L_{OA}	D	1	$D+1$
L_{S}	$D(30+3)$	$4(L_0+1)+6$	$33D+4L_0+10$
L_{UC}	$8D$	$1+(L_0+1)$	$8D+L_0+2$
L_{CC}	$7D$	L_0+1	$7D+L_0+1$
P	8	L_0	8

where:
N - filter order, D - number of previous sections, L_0 - last section order and $D = N + 6 - B$. If N div $6 = 0$ then $B = 1$ else $B = 0$; $L_0 = N - 6D$, $L_0 < 6$.

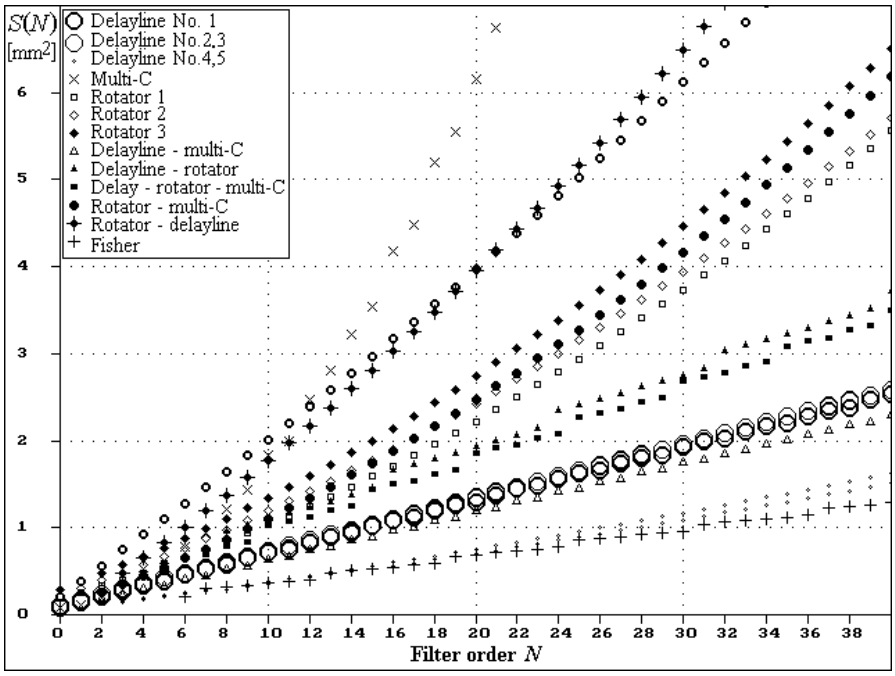


Figure 3.2: Chip areas for 3 μm CMOS technology

3.1.3 Conclusions

The estimated chip areas are presented in Figures 3.2, 3.3, 3.4, as functions of the filter order N for 3 μm, 2 μm and 0.8 μm CMOS technologies, respectively, and for SC FIR filter structures described in the second Chapter of this dissertation.

If we improve the technology, the area of particular elements will decrease but not linearly along with the technology parameters. In consequence, the entire chip area will decrease. The greatest area change can be noted for OA's (3.7 : 1 for the change from 3 μm to 0.8 μm CMOS technology). Intermediate changes

can be observed for switches (3.33 : 1). The change of the area of capacitors is smaller, i.e., about 1.8 : 1. In consequence the highest progress appears in these structures, which comprise larger numbers of OA's (rotator, delay lines No. 1, No. 2, No. 3) and smaller numbers of capacitors. Thus some structures, which from the perspective of chip area are preferable in one technology, are not such in the other technology. For example, the chip area of a multi-C structure (N=20) is equal to 6.2 mm^2 for 3 μm CMOS technology but 2.9 mm^2 for 0.8 μm CMOS technology. It means that the chip area can be decreased by 2.1 : 1. For the rotator structure this ratio is greater. It equals 3.2 : 1. The rotator structure comprises a large number of OA's and, therefore, the improvement is bigger than in the case of the multi-C structure, which comprises a large number of capacitors but only a single OA.

A vast scope of freedom exists as far as the design of composite structures is concerned. A filter of order N can be realized in many different ways, e.g., the order of the rotator-delay line structure is given by $N = M + L$. One of the values M and L can be treated

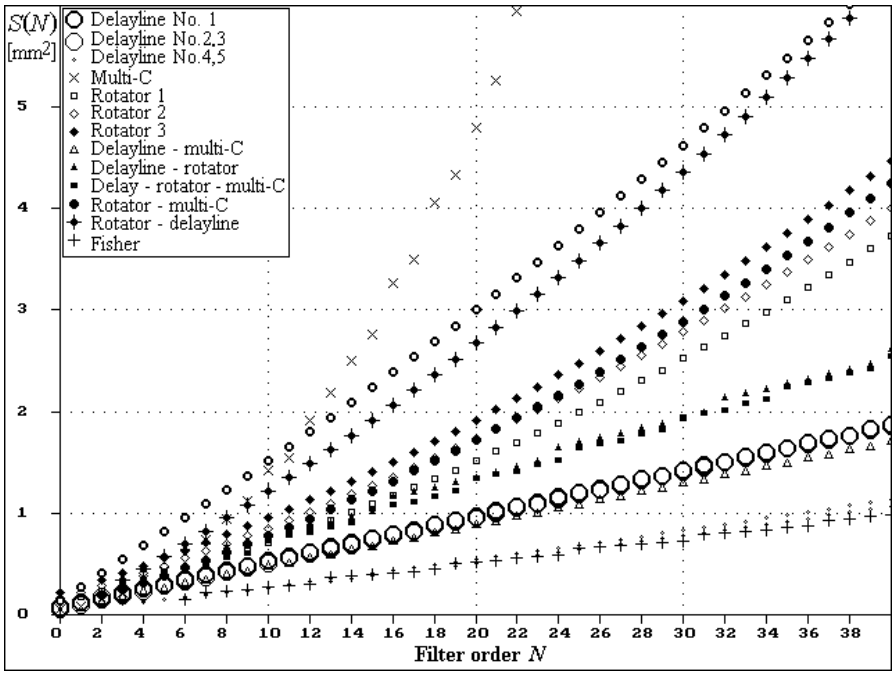


Figure 3.3: Chip areas for 2 μm CMOS technology

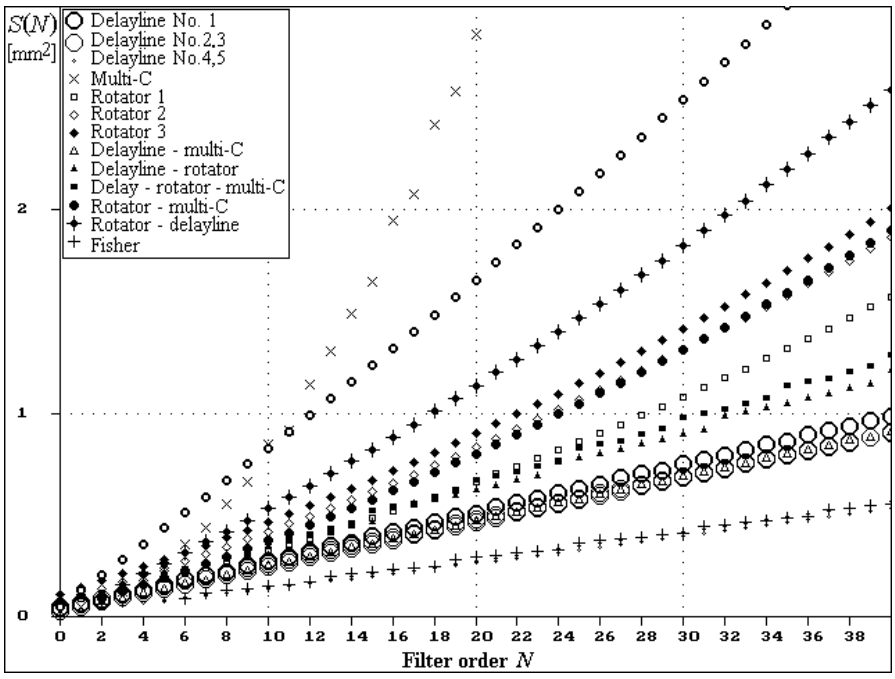


Figure 3.4: Chip areas for 0.8 μm CMOS technology

as a parameter. The chip area will in every case be different. To evaluate the optimal chip area, function $S = f(M, L)$ must be calculated to find the best partition of N to M and L.

3.2 Evaluation of the chip area on the basis of the real values of SC FIR filter coefficients

In this Section we present an improved method of evaluating the chip area. The method presented in the last subsection has an important disadvantage, which is the constant value of the area of the coefficient capacitors. In practice the chip area of these elements depends on the frequency response of the filter. When the spread of the values of the filter coefficient is high, then the total area of all coefficient capacitors is also very high. In the next part we present two extreme cases of the frequency responses. One is the filter with all equal coefficient values, and the second is the Butterworth (flat) filter with big dispersion of the values of the filter coefficients. When the filter order N is high and, additionally, the dispersion between coefficients is high (like in the Butterworth filter), then the total chip area of the filter is very high. In results such filters as whole are not realizable in the SC technique.

Because of this, a new method based on the filter decomposition into sections was proposed to solve this problem. It is presented in the following Subsection. At the end the obtained results are presented.

3.2.1 Influence of the frequency response of the filter on the chip area

In the SC FIR filters, coefficients are realized as ratios of capacitors in the input branches of the summer circuit (the coefficient capacitors) to the capacitor in the feedback of the operational amplifier at the output of the summer circuit. These coefficient capacitors (CC's) are built with tiny unit capacitors (UC's) connected in parallel. In practice, the coefficient with the smallest value is represented by a single UC. Other coefficients contain more than one UC, proportionally to their values. In the case of a high spread of the filter coefficients, the largest CC needs a lot of UC's and, in consequence, the total number of UC's (and the whole chip area) is high.

Figure 3.5 shows frequency responses of two illustrative low-pass filters. The first one (Fig. 3.5a) is the Butterworth filter and the second one (Fig. 3.5b) is the DFT-type filter. In the first case, the coefficients of the filter of order N are determined by the N'th row in the Pascal triangle (Fig. 3.6) in such a way that each coefficient (corresponding to a particular position in this row) is divided by the sum of all coefficients in this row. Thus, the greater the filter order N, the greater is the coefficient spread. In the second case no spread occurs because all coefficients are equal. For instance, for

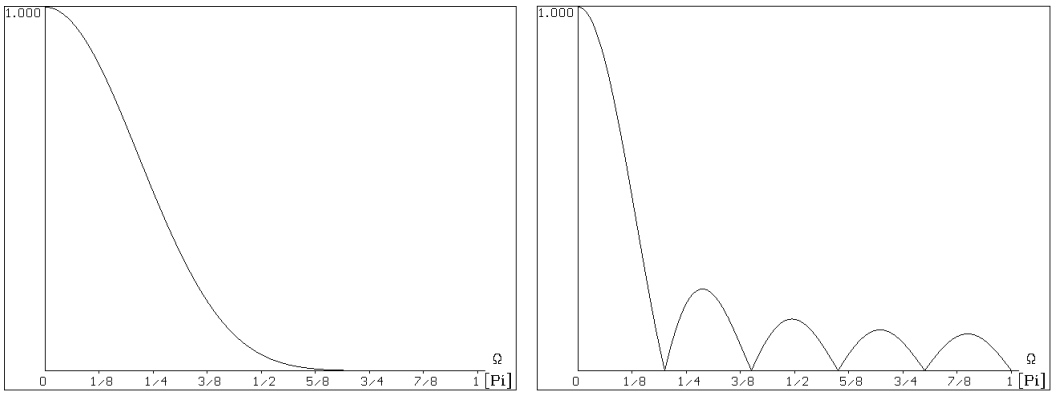


Figure 3.5: Frequency responses of the illustrative low-pass filters: (a) Butterworth (flat) filter ($N = 9$), (b) DFT-type filter (all coefficients h_i are equal) ($N = 9$)

N=1	1 1
N=2	1 2 1
N=3	1 3 3 1
N=4	1 4 6 4 1
N=5	1 5 10 10 5 1
N=6	1 6 15 20 15 6 1
N=7	1 7 21 35 35 21 7 1

Figure 3.6: The Pascal triangle

the Butterworth filter of order $N = 9$ we need the coefficients

$$\{h_i\} =$$

$$\{0.00195; 0.01758; 0.07031; 0.16406; 0.24609; 0.24609; 0.16406; 0.07031; 0.01758; 0.00195\}\,.$$

These values are characterized by a quite large spread of about 128.

It can be shown that the total area of capacitors $S_{\mathrm{CT}}(N)$ required for the integration of the Butterworth filter of order N, if realized directly using the delay-line structure No. 2 or No. 3, is given by the following equation

$$S_{\mathrm{CT}}(N) = \frac{2}{h_{i\min}} S_{\mathrm{CM}} = 2^{N+1} S_{\mathrm{CM}}\,, \tag{3.3}$$

where: N – filter order, $h_{i\min}$ – the minimal coefficient h_i, S_{CM} - area of the minimal capacitor (it should be a multiple of the unit capacitor area S_{UC}). Assume, for example, that $S_{\mathrm{CM}} = 3800\ \mu\mathrm{m}^2$ then for $N = 40$ we would get $S_{\mathrm{CT}} \approx 8400\ \mathrm{m}^2$, which is obviously an absurd result.

In the multi-C structure (Fig. 2.12) each signal sample is stored in an individual capacitor. Because of this each coefficient h_i is composed of several capacitors and

therefore the number of capacitors increases very fast with the filter order N. This results from the fact that the number of coefficient capacitors (CC's) in each coefficient h_i is equal to at least i and is given by the following formula

$$L_{h\mathrm{CC}}(i,N) = i + 1 + (N+1) \bmod (i+1)\,, \tag{3.4}$$

where: N – filter order, $i = 0, \ldots, N$, and "mod" means the remainder in the natural division.

The total number of capacitors in the multi-C structure is given by the equation

$$L_{\mathrm{CC}} = \frac{(N+2)(N+1)}{2} + \sum_{i=0}^{N} (N+1) \mathrm{mod}\,(i+1)\,. \tag{3.5}$$

In the multi-C structure there is a single OA ($L_{\mathrm{OA}} = 1$), about $3L_{\mathrm{CC}}$ S's ($L_{\mathrm{S}} = 3L_{\mathrm{CC}}$), and $L_{\mathrm{UC}} = 0$.

For the Butterworth filter realized with the multi-C structure the appropriate equation for the total area of capacitors ($S_{\mathrm{CT}}(N)$) is as follows

$$S_{\mathrm{CT}}(N) = \sum_{i=0}^{N} (L_{h\mathrm{CC}}(i,N) + 1) L_{h\mathrm{CM}}(i,N) S_{\mathrm{CM}}\,, \tag{3.6}$$

where: $L_{h\mathrm{CC}}(i,N)$ is given by equation (3.4), $L_{h\mathrm{CM}}(i,N)$ is the number of minimal capacitors with area S_{CM} in each of the CC's in a particular coefficient h_i. $L_{h\mathrm{CM}}(i,N)$ can be computed by the recursive formula

$$L_{h\mathrm{CM}}(i,N) = 1 \quad \text{for} \quad i = 0 \quad \text{and arbitrary} \quad N\,;$$

$$L_{h\mathrm{CM}}(i,N) = L_{h\mathrm{CM}}(i-1, N-1) + L_{h\mathrm{CM}}(i, N-1) \quad \text{for} \quad 0 < i < N\,. \tag{3.7}$$

The additional term $+1$ in the Equation (3.6) results from the fact that the feedback capacitor has the same area as the sum of all capacitors in coefficients h_i.

The second case (Fig.3.5b) is the DFT-type filter, i.e., that, whose all coefficients are equal. It is obviously the most convenient case for the realization as an integrated circuit. For instance, in the case of $N = 9$, $h_i = 0.1$, $i = 0, 1, \ldots, 9$. In result, the total capacitor area $S_{\mathrm{CT}}(N)$ rises linearly with the filter order N according to the equation (3.8) valid for the delay-line structures No. 2, and No. 3 and according to the equation (3.9) for the multi-C structure.

$$S_{\mathrm{CT}}(N) = 2(N+1) S_{\mathrm{CM}}\,, \tag{3.8}$$

$$S_{\mathrm{CT}}(N) = 2 \sum_{i=0}^{N} (L_{h\mathrm{CC}}(i,N) + 1) S_{\mathrm{CM}}\,. \tag{3.9}$$

Equation (3.9) is a special case of equation (3.6) with $L_{hCM}(i, N) = 1$ for all i and N. It is worth noting that from equation (3.6) we can obtain the same result as from equation (3.3) if $L_{hCC}(i, N) = 1$ for all i and N (for the delay line structures No. 2 and No. 3).

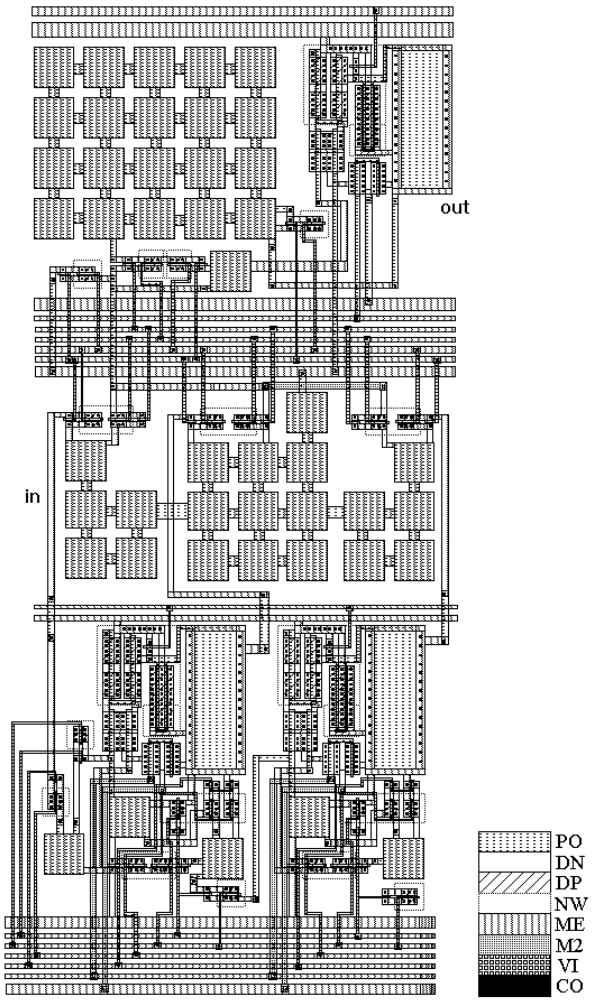


Figure 3.7: Layout of the section with the delay-line structure No. 3 ($N = 2$)

The above considerations and examples show that the integration of an SC FIR filter, whose transfer function is directly (i.e., as a whole) realized, has a limited range of use. We propose two different approaches to overcome this serious difficulty:

- a cascade decomposition of the whole filter transfer function into sections of the second order (and possibly into a single first order section if the filter order is odd),
- a polyphase decomposition of the transfer function and the use of the composite structures [1, 33].

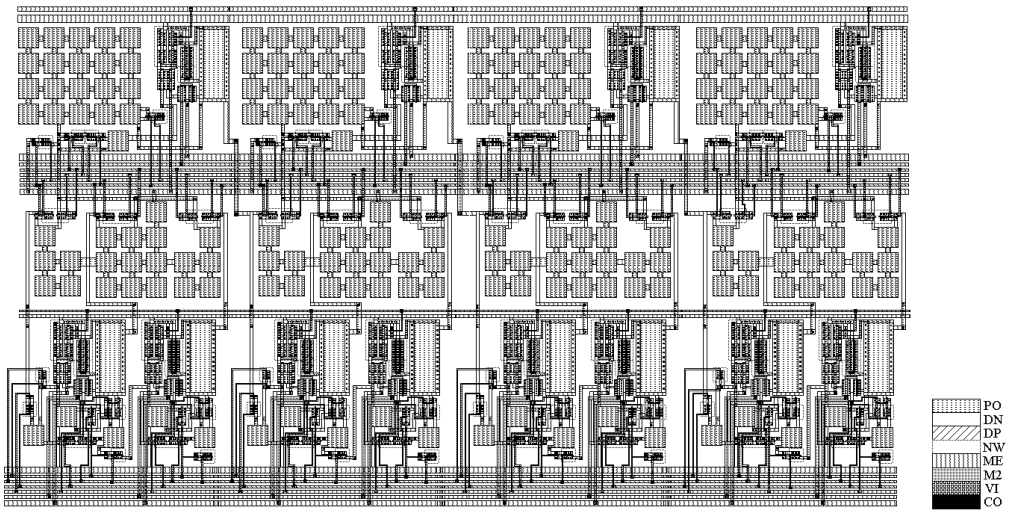


Figure 3.8: Layout of the composite (cascade) delay-line structure No. 3 ($N = 8$)

Both solutions are characterized by many additional advantages. Among the most important are:

- modular structure,
- reduced number of clock phases (in some cases only),
- simpler layout and the reduced chip area,
- increased frequency range,
- lower sensitivity.

The cascade decomposition significantly simplifies the realization of the FIR Butterworth filters, because in this case we can use identical second order sections with coefficients $\{h_i\} = \{0.25; 0.5; 0.25\}$ (Fig.3.7) and possibly a single first order section with coefficients $\{h_i\} = \{0.5; 0.5\}$. As an example, the cascade realization of the FIR Butterworth filter of order 8 is shown in 3.8. The circuits shown in Figs.3.7 and 3.8 have the following dimensions: $980 \times 420\,[\lambda]$ and $980 \times 1750\,[\lambda]$, respectively, ($1\,\lambda = 0.6\,\mu$m for 1.2 μm CMOS technology).

Cascaded delay-line structures possess important advantages:

- a simple two-phase (or four-phase) clock,
- possibility for partial outputs after each section,
- high modularity.

There are, however, also some disadvantages:

- larger number of active and other elements,
- accumulation of the rewrite errors,
- additional delay of $z^{-0.5}$ per section (if the recharge summers are used).

Delays introduced by the second order sections comprising the recharge summers give rise to a need for two types of such sections: the even and the odd section. Sections of these two types have to be interleaved in the filter structure. The presence of the additional delay makes it difficult to use these sections in adaptive systems, as in such case no displacement between the plant output and the adaptive filter output is allowed.

For FIR Butterworth filters the total area of capacitors in summers of all sections can be determined by the following formula

$$S_{\mathrm{CT}}(N) = 8S_{\mathrm{CM}}(N \operatorname{div} 2) + 4S_{\mathrm{CM}}(N \bmod 2)\,, \tag{3.10}$$

where: "div" means the natural division without rest. The number of Gillingham delay elements in the cascade realization does not change in comparison to the direct realization and equals $N-1$. The number of OA's in the summer circuits is, however, higher and equals

$$L_{\mathrm{OA}}(N) = N \operatorname{div} 2 + b\,, \tag{3.11}$$

where

$$b = \begin{cases} 1 & \text{for odd } N \\ 0 & \text{for even } N\,. \end{cases}$$

In the example projects, presented in the Fig.3.7 and 3.8, switches are realized as transmission gates, because of a small and almost constant on-resistance in contrast with switches realized as a single transistor. This, however, complicates the control of switches: two complementary clock signals (instead of a one) are necessary to control a single switch. This results in turn in the increment of the chip area, because the real number of clock phases (and also of respective connections) is doubled, i.e., is equal to 4 and not to 2.

The capacitors in the layouts presented in this subsection are realized as two plates: metal (ME) and polysilicon (PO) [5]. CC's are realized as parallel connections of many UC's. This makes it possible to keep the area-to-perimeter ratio constant [1].

3.2.2 Chip area evaluation

The method for the approximate (theoretical) evaluation of the chip area, presented in Section 3.1 is based on the assumption that the area parameters S_{OA}, S_{UC}, S_{CC}, and S_{S} in the equation (3.1) are constant. In practice, this assumption is usually not exactly true. For instance, parameter S_{CC}, which describes the area of the average coefficient

Table 3.14: Number of elements in cascaded delay-line structures

Element	Formula
OA	$L_{\mathrm{OA}} = 3(N \text{ div } 2) + 2(N \text{ mod } 2)$
UC	$L_{\mathrm{UC}} = 5(N \text{ div } 2) + 3(N \text{ mod } 2)$
CC	$L_{\mathrm{CC}} = 4(N \text{ div } 2) + 3(N \text{ mod } 2)$
S	$L_{\mathrm{S}} = 24(N \text{ div } 2) + 16(N \text{ mod } 2)$
No. of phases	$P = 2$

capacitor, depends on the type of the filter frequency response and increases with the filter order N according to the following equation

$$S_{\mathrm{CC}}(N) = \frac{S_{\mathrm{CT}}(N)}{L_{\mathrm{CC}}(N)}\,. \tag{3.12}$$

For the delay-line structure No. 3 we get

$$S_{\mathrm{CC}}(N) = \frac{2(N+1)S_{\mathrm{CM}}}{N+2} \approx 2S_{\mathrm{CM}} \tag{3.13}$$

in the case of the DFT-type filter (i.e., for all coefficients h_i equal to each other) and

$$S_{\mathrm{CC}}(N) = \frac{2^{N+1}S_{\mathrm{CM}}}{N+2} \tag{3.14}$$

in the case of the Butterworth filter. The respective equations for the delay-line structure No. 2 are similar.

These two extreme examples show that the formulation of the chip area as a function of the filter order N only (i.e., as a single curve for the given order N) is not possible, because of a very high dispersion of S_{CC}. In cascaded delay-line structures, however, this dispersion is much smaller. For Butterworth filters we even get a very simple relation $S_{\mathrm{CC}} = 2S_{\mathrm{CM}}$.

For the cascaded delay-line structures equations for computation of numbers of basic elements as functions of the filter order N are listed in Table 3.14. Constant coefficients occurring with expressions $(N \operatorname{div} 2)$ and $(N \bmod 2)$ in Table 3.14 follow from equations given in Table 3.2 for $N = 2$ (second order section) and $N = 1$ (first order section), respectively.

The analysis presented so far still can be only used for the approximate evaluation of the chip area. It is due to the following facts:

- it is necessary to add some empty place between particular elements in the chip layout,
- we must remember that in reality we use the clock with complementary phases (i.e., with a doubled number of phases); this increases the required chip area,

- some parts of the chip area must be used for connections of the power supply and of the control signals such as V_{DD}, V_{SS}, V_{ACT} and others,
- it is important to fulfil the design rules required for a particular technology: minimal layer dimensions, and spacing between particular layers exist, which have to be taken into account during the design process and cannot be omitted in the evaluation of the required chip area; in result, the clock path in reality is wider than that estimated in the third section,
- because CC's are realized as parallel connections of UC's, the area of a CC is a bit larger than that equal to the product of the UC area by the number of UC's – it is because of some empty place necessary to leave between UC's.

It should also be stressed that if spacing between layers is too small, then the parasitic capacity will be unacceptably high. This also influences the required chip area.

For the cascaded delay-line structures the total (approximated) chip area can be computed using the following equation

$$\begin{aligned} S(N) = (3S_{\mathrm{OA}} + 4S_{\mathrm{CC}}(2) + 6S_{\mathrm{UC}} + 26S_{\mathrm{S}} + PS_{\mathrm{C}}(2))(N \operatorname{div} 2) + \\ +(2S_{\mathrm{OA}} + 3S_{\mathrm{CC}}(1) + 4S_{\mathrm{UC}} + 17S_{\mathrm{S}} + PS_{\mathrm{C}}(1))(N \bmod 2)\,. \end{aligned} \tag{3.15}$$

Coefficients $S_{\mathrm{C}}(1)$ and $S_{\mathrm{C}}(2)$ result from equation (3.2) for $N = 1$ and $N = 2$, respectively. Their estimates are: $S_{\mathrm{C}}(1) = 840\ \mu\mathrm{m}^2$ and $S_{\mathrm{C}}(2) = 1080\ \mu\mathrm{m}^2$. Coefficients $S_{\mathrm{CC}}(1)$ and $S_{\mathrm{CC}}(2)$ should be computed according to equations (3.13), (3.14) for $N = 1$ and $N = 2$, respectively.

The plots of the chip area are depicted in the Figures 3.9 and 3.10 as functions of the filter order N for the delay-line structure No. 3 and for the multi-C structure, respectively. We do not present the results for the delay-line structure No. 2 because the chip area is in this case approximately equal to that obtained for the delay-line structure No. 3. Different curves are plotted and compared, including the approximated chip estimations described in Section 3.1 and the exact chip evaluation of real filters. The Butterwoth (flat) filters and the DFT-type (uniform coefficient filters) are treated as two "extreme" cases. Filters with uniform coefficients always require the smallest chip area because of no coefficient spread. In result, all coefficient capacitors (CC's) are small. For the flat filters, however, the coefficient spread is the highest among the cases considered and, in result, the chip area is the largest obtained. Thus, the characteristics of SC FIR filters of practical relevance lie inside the area between these two "extreme" curves.

In Figure 3.9 two additional, interesting curves are shown, corresponding to the cascade realization of the Butterworth filter (i.e., to the realization of the whole filter circuit as a cascade of second order sections and possibly of a single first order section occurring if the filter order is odd). The first curve is obtained by the approximate estimation using equation (3.15). The second one is exact and corresponds to the realization of

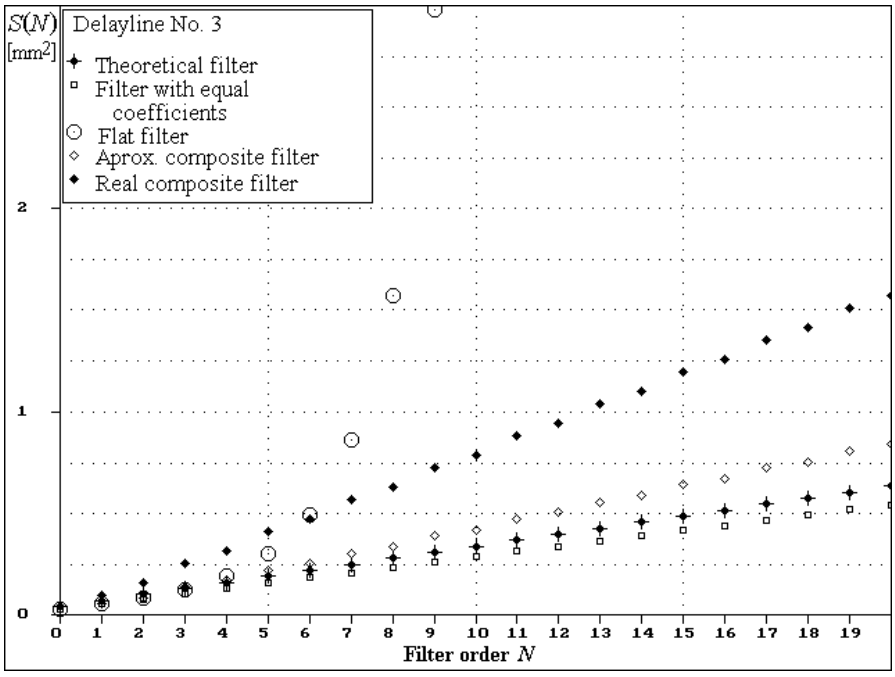


Figure 3.9: Chip area curves for the delay-line structure No. 3

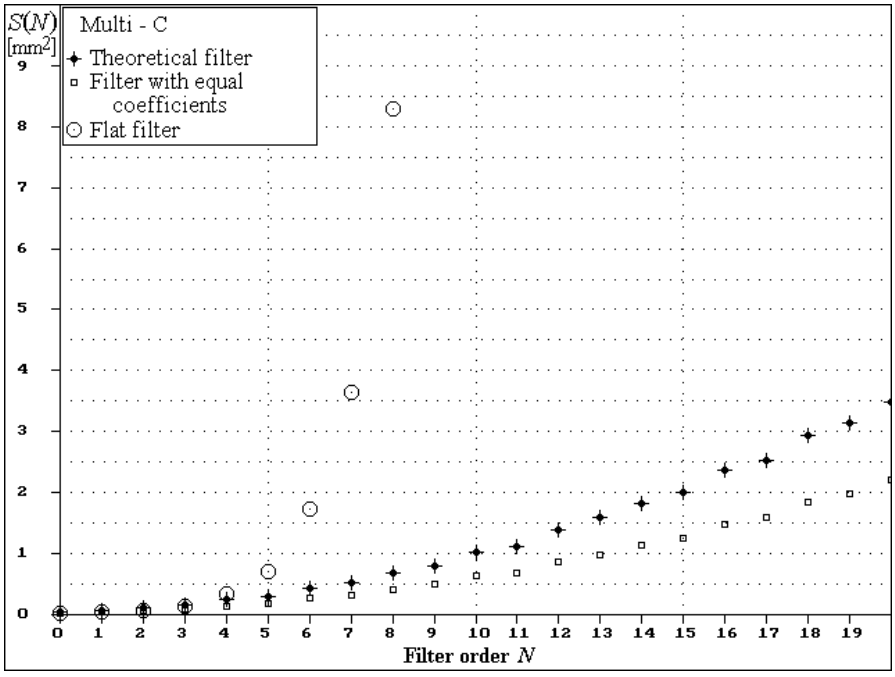


Figure 3.10: Chip area curves for the multi-C structure

the integrated circuit. By the analysis of curves in Fig.3.9 it can be concluded that the cascade structure is the only reasonable solution for the FIR filters with a large coefficient spread, e.g., for the considered Butterworth filters. In contrast, for filters with uniform coefficients, the smallest chip area can be obtained using the direct delay-line structures.

3.3 Comparison of the SC FIR filter structures on the basis of the clock system criteria

3.3.1 Theoretical clock systems for particular SC FIR filters

In this Subsection theoretical clock systems for particular basic SC FIR filter structures are studied and evaluated. The word "theoretical" means that we do not take all practical aspects into account of the realization of a clock system. In practice, there exist various difficulties, which cause that the clock system is more complicated than in the theory. These aspects are considered in the next Subsection. Simplified (theoretical) analysis, given here, is an essential and indispensable basis for further analysis towards practical realization.

Delay line structure with Gillingham delay elements (No. 3)

In this case only two clock phases are needed. An important advantage is that the number of the clock phases does not depend on the filter length N [1, 2, 33]. The clock system is very simple (see Figures 2.9 and 3.11). All switches in the structure are driven by only one clock phase.

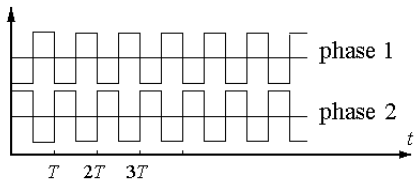


Figure 3.11: Clock control in the delay line structure No. 3

Delay line (Fisher) structure (No. 4)

In this structure (see Figure 2.10) the number of clock phases is given by equation (3.16). It can be seen that this value depends on the filter order N. In structures of this kind, each clock phase must occur during the processing of a single sample.

The result is that the greater the filter order N, the better must be OA's dynamics to preserve the maximum frequency range. Additional problem is the availability of the output samples through $1/(N-2)$ of the sampling period only, unless a storage element at output (e.g., a capacitor or a sample & hold element) is used [1, 2, 33].

$$L_{\mathrm{P}} = 2(N+1), \text{ where } N - \text{ filter order}. \tag{3.16}$$

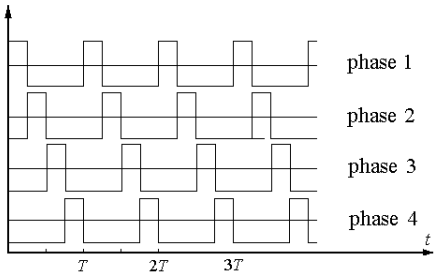


Figure 3.12: Clock control in the delay line structure No. 4 for $N = 2$

Delay line structure with even-odd delay elements (No. 1)

In this case we need a four-phase clock but the number of clock phases does not depend on the filter order N [1, 2, 33]. An additional problem is that a part of the switches in the structure is driven by two different clock phases — a fact which creates the problem of separation of the clock phases. In Figure 3.13 one can see all combinations of the clock phases needed to drive the even-odd delay line structure (Figure 2.7).

Rotator structure

In this case the number of clock phases is given by equation (3.17). In structures of this kind only two clock phases must occur during processing of a single sample (in contrary to the delay line structure No. 4). In consequence, the upper frequency range does not depend on the number of clock phases and on the filter order N [1, 2, 33]. In Figure 3.14 the clock control for $N = 2$ is presented.

$$L_{\mathrm{P}} = N + 3, \text{ where } N - \text{ filter order } . \tag{3.17}$$

Parallel (multi-C) structure

This structure has a very important advantage — namely that the sample error does not accumulates along the filter structure, which happens in the delay line structures. However, we pay for this advantage with a relatively complicated clock. Theoretically,

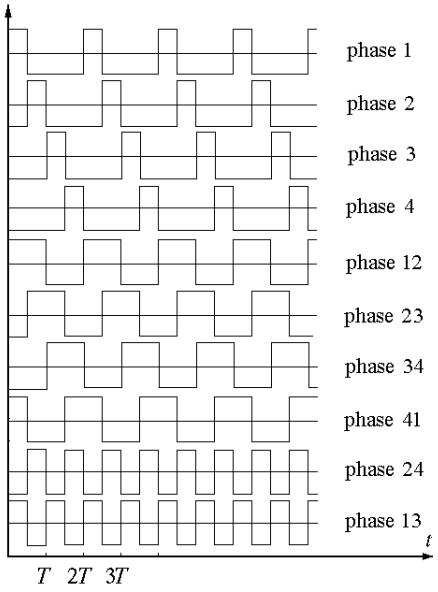


Figure 3.13: Clock control in the delay line structure No. 1

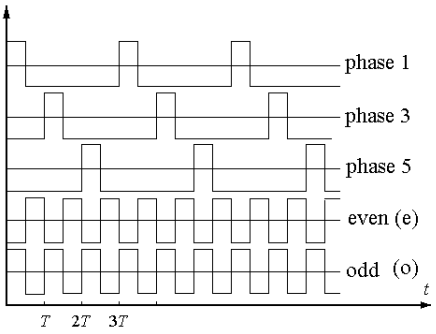


Figure 3.14: Clock control in the rotator structure for $N = 2$

the number of clock phases is given by equation (3.18). This value grows considerably with the filter order N but only two clock phases are needed during the processing of a single sample [1, 2, 33].

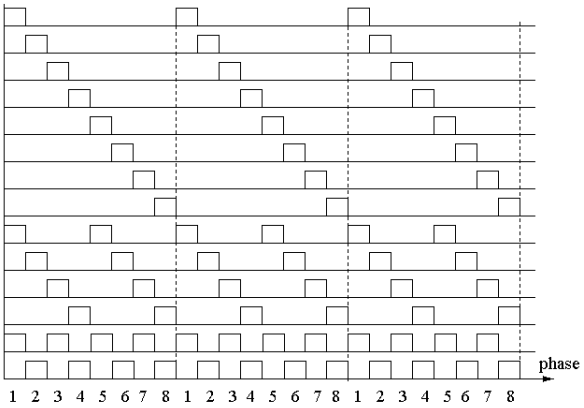


Figure 3.15: Clock control in the multi-C structure for $N = 3$

$$L_{\mathrm{P}} = 2(N+1), \text{ where } N - \text{ filter order } . \tag{3.18}$$

In the multi-C structure presented in Figure 2.12 we see that switches are driven by more than one clock phase, and additionally, these combinations are different for almost each single switch. The problem of separation of clock phases is in this case practically the most complicated among all SC FIR filter structures. In Figure 3.15 clock control of a multi-C structure for $N = 3$ is presented.

3.3.2 Practical aspects of realization of clock systems

In practice, the number of clock signals may be, for particular structures, greater than the one given in the last Subsection. There are some reasons for this.

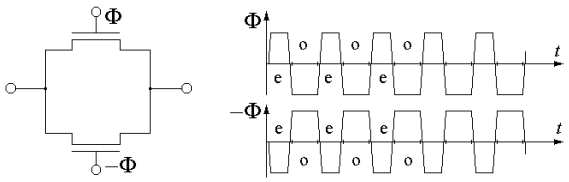


Figure 3.16: Transmission gate and a complementary clock

The first problem consists in the use of switches built not as single MOS transistors but as transmission gates, i.e., as parallel connections of an NMOS and a PMOS transistor. This solution is used because although the on-resistance of a single n-type and p-type transistor varies drastically as a function of the drain-source voltage, the transmission

gate on-resistance varies rather moderately, in the range of 10 kΩ to 25 kΩ. Thus, a clock with complementary phases is needed (Figure 3.16) and the number of clock signals is doubled [1, 5, 8].

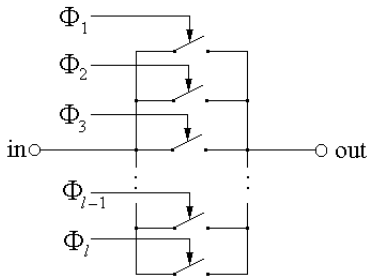


Figure 3.17: Parallel connection of switches

Another problem occurs in those structures, in which particular switches must be controlled by more than a single clock phase. These are for example basic structures such as the delay line structure No. 1, multi-C structure, and various composite structures built on such a basis. For example: the delay line - rotator structure, the delay line - multi-C structure, the delay line - rotator - multi-C structure. All switches controlled by a single clock phase are connected to a single layout path (metal or polysilicon).

If we want to control a particular switch by two different clock phases, we cannot simply connect both corresponding clock paths to this switch (to the gate of a MOS transistor) because all other switches connected to these two paths would be controlled by these both clock phases either. Thus we have to search for some way to separate layout paths. Solutions of this problem are suggested and analyzed below.

Parallel connection of switches

In his solution we use parallel switches. It is necessary to connect in parallel as many transmission gates (or single MOS transistors) as many different clock phases are needed (Figure 3.17). Each transmission gate in such a parallel connection is controlled by a pair of complementary clock signals (Figure 3.16). This solution is usable in those structures, in which moderate numbers of clock phases control switches, e.g., for the delay line No. 1. In this structure the maximum number of clock phases connected to a single switch is equal to two. In other cases, especially for multi-C structures, the number of transmission gates would grow unacceptably with the filter order N. It is given by equation (3.19)

$$L_{\mathrm{S}} = 3\frac{(N+2)(N+1)}{2} + 3\sum_{i+1}^{N}(N+1) \bmod (i+1) + 1\,. \tag{3.19}$$

The number of switches will be higher by about 40%. In consequence the enlargement of the chip area will occur. An additional disadvantage follows from the fact, that each

of such switches is controlled by a great number of clock phases. This complicates the local layout structure. Yet, this solution has also a very important advantage. It enables us to use a simple clock with the minimum number of clock phases. The theoretical number of clock phases is preserved or multiplied by two (for transmission gates). This advantage is especially important for an external multiphase clock.

Enlargement of the number of clock phases

Using this solution it is necessary to find all switches, for which an unrepeatable combination of clock phases exists. Then we have to implement each of such combination on a separate layout path, i.e., as an additional clock signal. This solution has, however, a serious disadvantage, which follows from the fact, that for some SC FIR filter structures, for various filter orders construction of the clock circuit is unique, i.e., a small modification in the filter circuit (e.g., change of the order N) will cause the change of the whole clock layout. This difficulty can be overcome by a programmable structure, which will be able to be fitted in a simple way to particular cases. This solution can be reasonable for structures with a small number of combinations of clock phases.

For the multi-C structure the number of combinations of clock phases C_{C} is given by equation (3.20)

$$C_{\mathrm{C}} = 2(N+1) + \frac{(2+2((N+1)\ \mathrm{div}\ 2))((N+1)\ \mathrm{div}\ 2)2}{2}\,. \tag{3.20}$$

In Figure 3.15 a clock control diagram for a multi-C structure for the case of $N = 3$ is shown. In this case the number of different combinations of clock phases is equal to 14. For filter of 11th order the number of combinations C_{C} is equal to 66. This shows that for multi-C structures the considered solution can be used only for filters of relatively low orders. It is different in the case of the delay line structure No. 1 with even-odd delay elements. In that case the number of different combinations of clock phases is equal to 10 (see Figure 3.13) and does not depend on the filter order N. Because of a great number of different clock signals this solution is preferable rather for structures with the internal clock layout.

Switching circuit

This is a circuit, which connects chosen clock patches to particular switches at a certain moment. This solution enables us to use a simple clock, in which phases are placed regularly (c.f., Figure 3.12 a clock for the delay line structure No. 4). The patches with clock phases should be placed around the circuit. In particular (local) circuit areas, in which an appropriate set of clock signal is needed, a special circuit should be implemented to provide this set of clock phases. The simplest way to arrange such a circuit is to use OR gates, which separate particular phases from each other. An illustrative circuit for the multi-C filter structure of order $N = 3$ is shown in Figure 3.18.

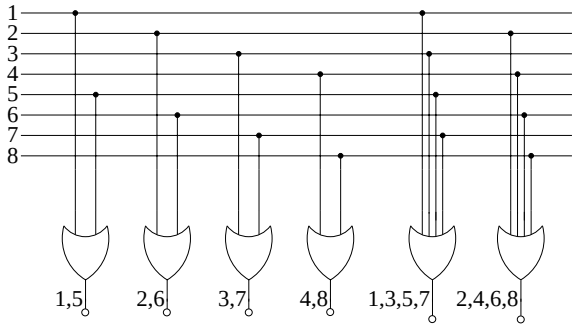


Figure 3.18: Combinatory circuit for multi-C structure $N = 3$

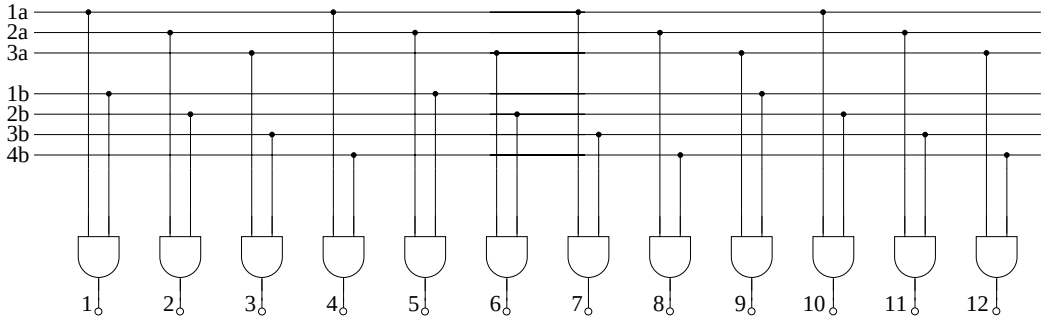


Figure 3.19: Circuit for enlargement of the clock phases

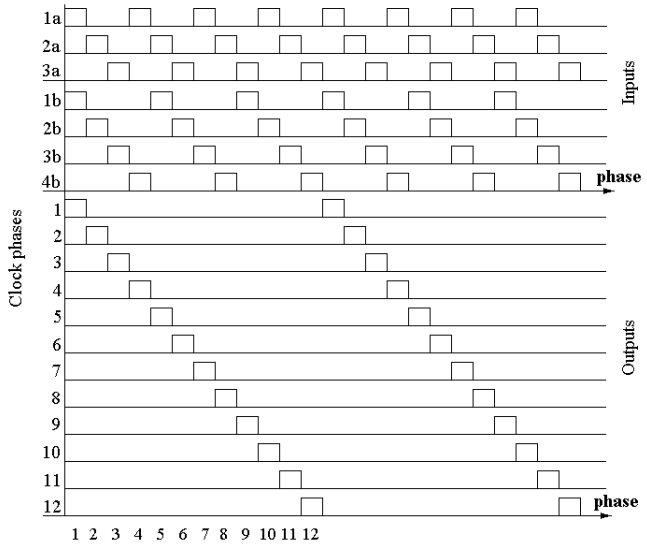


Figure 3.20: Clock diagram for the circuit in Fig. 3.19

The phases cannot be short-circuited, but the control of particular switches with more than a single clock phase is necessary. If separation gates are used, their output signals can be closed together in different ways and the phase connections are local. This solution makes it possible to obtain any combination of the clock signals, which is needed. Naturally, it is necessary to remember that the output signals are distorted beyond the gates to a certain degree. However, although the SC FIR filters (some structures) in general do not need perfect shapes of the clock signals, particular clock phases must cross in such a way as to avoid the situation, in which all switches are simultaneously opened. CMOS realization of the clock systems based on this principle is presented in Section 4.3.

Internal enlargement of the number of clock phases

In some of the above structures the number of clock phases increases if the filter order N increases. Such situation is not desirable, especially when an external clock circuit is used. To provide an appropriate number of clock signals, it would be necessary to enlarge the number of pins. This obviously limits the maximum realizable filter order and enlarges the area of the integrated circuit. To overcome this problem we can use a solution, which is based on the principle described in the previous Subsection. To obtain more clock phases it is necessary to use a special combinatory circuit, which can be realized with AND gates. The combinatory circuit needs two sets of the clock systems. Signals from one set are connected to the first inputs of the AND gates. Signals from the second set are connected to the second inputs of the AND gates. In this way we obtain a new set of clock signals at the outputs of the gates. This principle is illustrated in Figure 3.19, in which, by crossing signals of the three-phase clock set with the four-phase clock set, we obtain a twelve-phase clock at the output. The diagram of clock phases in the circuit is shown in Figure 3.20. This solution is very convenient in use, yet, it also has some disadvantages. The problem is that we cannot obtain arbitrary numbers of clock signals. This is the result of the fact that it is reasonable to cross only such clock signal sets, of which the number of phases has a common, sufficiently high multiple. If we cross for example two sets with the number of phases equal to 6 and 4, we obtain at the output only a 12-phase clock, just like in the case of crossing two sets with phase numbers 3 and 4.

Various combinations of solutions

In realizations of integrated circuits, the solutions presented above can be connected. Different criteria may decide, on which combination will be used. One of them is certainly the chip area. All presented methods complicate the circuit, and thus enlarge the chip area. Because of this, it is necessary to fit particular methods to particular structures. A very interesting solution is to connect methods based on the principle of combinatory circuits. This enables us to realize a two stage combinatory circuit. In the first stage we enlarge the number of clock phases and in the second one we separate the clock phases.

3.4 Comparison of SC FIR filter structures on the basis of power consumption

Criterion of minimization of the power consumption is important if SC FIR filters are used in low-power circuits. The comparison of the structures on the basis of this criterion is in general quite simple, because the power consumption depends on the number of active elements (operational amplifiers - OA's) in the circuit. For this reason the multi-C structure as well as the delay line structures No. 4 and No. 5 are solutions with low power consumption, because they contain only one OA. The delay line structures No. 2 and No. 3 and the rotator structures contain a greater number of OA's, and the number of these elements is almost equal to the filter order. Due to this fact, these filters are solutions with relatively high power consumption. The even-odd delay line structures (No. 1) should be classified in the middle. Even and odd delay elements can store more than one signal sample, and for a given filter order the number of OA's is lower than in the delay line structures No. 2 and No. 3. A family of the even-odd delay line structures is analyzed in detail in Section 3.6. In general, the criteria of the power consumption, although important can be minimized by optimization of OA's (c.f., Chapter 4).

3.5 Comparison of SC FIR filter structures on the basis of signal quality

Criteria defining the required signal quality are especially important, if high stopband attenuation is expected. All nonidealities in particular building elements of SC FIR filters are primarily visible in the stopband. The most important errors result from the read and write operations of signal samples, which are stored on capacitors in a delay line and in coefficients. In general, the higher the number of the read and write operations, the higher is the summarized error.

In all delay line structures the number of read and write operations is high and depends on the filter order. These structures must be designed very carefully to minimize the effect coupling with the rewriting operations (c.f., Chapter 4).

In the rotator structures and in the multi-C structure the number of read and write operations is low — equal to 1 or 2 only and is independent on the filter order. Because of this, these structures theoretically have the highest quality of the signal processing.

In the family of even-odd delay line structures, the number of read and write operations can by minimized by increasing the order of even and odd delay elements. This parameter designed by R is defined in Subsection 3.6.1.

Other source of nonidealities are various parasitics (especially capacities) in the integrated circuit. During the design process of the integrated circuit it is necessary to localize places, in which the parasitic capacities exert a substantial influence on the

signal. The final step is to place the most sensitive signal paths in such a way in the integrated circuit so as to minimize the influence of the parasitic capacities.

3.6 New family of even-odd delay line structures

In this Section we postulate a new family of the delay line structures with even and odd delay elements. This family has important advantages in comparison to other SC FIR structures, as was already discussed in previous Sections. The original even and odd delay elements proposed in [3] are here referred to as the first order R. Now we are going to propose and analyze also even and odd delay elements of higher orders.

In the next Subsection we present a conception of the tapped delay lines and consequently of the FIR filters composed of higher order even and odd delay elements. Then we analyze the required chip area for the proposed filter architectures for various filter frequency responses. Two cases are similar to those analyzed in Section 3.2, i.e., a filter with equal coefficients (the DFT filter) and the flat passband (Butterworth) filter. In considerations an illustrative example is used, namely the GSM channel filter, which is described analyzed in Chapter 4.

3.6.1 Even and odd delay elements

The even delay (memory) elements offer (write) stored signal samples at even clock phases but they register (read) them at odd phases. Complementary (odd) elements operate just in an opposite way and therefore they should be connected alternately with even elements in a delay line. A multiphase clock that controls operation of these elements must have an even number of clock phases $k \geq 2$. Both (even and odd) elements store samples for an odd number of clock phases, equal to $(k-1)$. A number R defined as $R = k/2-1$ is called the even-odd element delay order. Even and odd elements of zeroed order are identical [3] and offer an extremely simple two-phase delay line. They are, however, not offset compensated and, therefore, they will not be considered here.

First order even and odd delay elements

The 1'st order even and odd delay elements are presented in the Figures 3.21 and 3.22, respectively. They contain two storage capacitors only and are controlled with a four phase clock. A principle of their operation is explained below. It is the same principle which was applied to elements of higher orders.

In the Figure 3.23 two possible states of operation of the even and odd delay elements are shown. The read state (a) occurs at odd clock phases for an even element and at even clock phases for an odd element. The write state (b) occurs just in opposite clock phases. The voltage U_x is given in these states by equations, respectively:

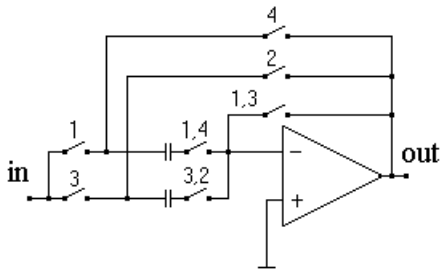


Figure 3.21: 1'st order even delay element

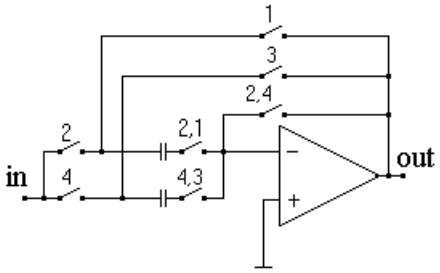


Figure 3.22: 1'st order odd delay element

$$U_x = U_{\text{in}}(n-3) - \frac{A}{1+A}U_{\text{off}}\,, \tag{3.21}$$

$$U_x = U_{\text{out}}(n)\frac{1+A}{A} - U_{\text{off}}\,. \tag{3.22}$$

Thus the output voltage equals

$$U_{\text{out}}(n) = \frac{1}{1+\frac{1}{A}}U_{\text{in}}(n-3) + \frac{A}{(1+A)^2}U_{\text{off}}\,. \tag{3.23}$$

We conclude from equation (3.23) that the considered elements are in practice offset-compensated, when the value of A is high. Note also that the output voltage U_{out} does not depend on the capacitor values, i.e., our delay elements are insensitive to capacitor mismatch, which is another important advantage of them.

Higher order even and odd delay elements

Even and odd delay elements of higher orders contain greater numbers of storage capacitors, and are driven by more complicated (multiphase) clock systems, as illustrated in Figures 3.24 and 3.25.

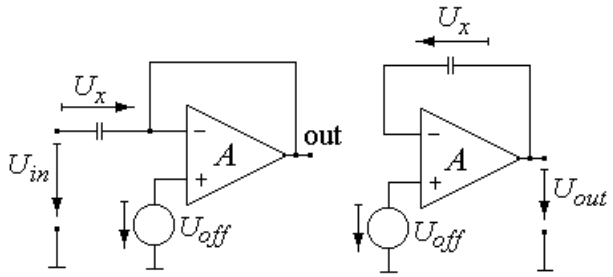


Figure 3.23: Operation of even and odd delay elements

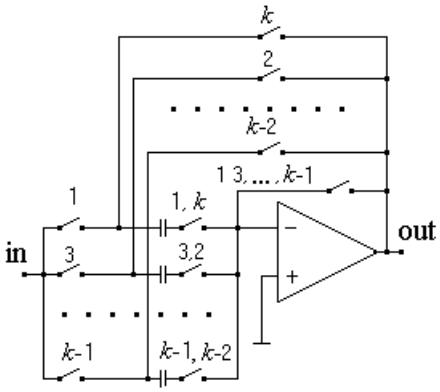


Figure 3.24: Higher order even delay element

Equations (3.21), (3.22), and (3.23) will still remain valid for higher order delay elements, if we replace voltage $U_{\text{in}}(n-3)$ by $U_{\text{in}}(n-k+1)$, where an even number k denotes the total number of clock phases. The delay between output and input is in this case equal to $k-1$ samples. The delay element order R is by definition related to the number of clock phases with the equation (3.24)

$$k = 2(R+1)\,. \tag{3.24}$$

Although the total number of clock phases increases with the even and odd delay element order R, the number of clock phases per one signal sample remains constant and is always equal to two. Thus OA's operate in the same conditions (independently from order R) and the maximum signal frequency remains constant.

It should also be stressed that we need an equivalent of approximately only $2/(k-1) = 2/(2R+1)$ OA's per one effective delay and this is the main advantage of higher order even and odd delay elements.

The number of switches L_{S} and the number of unit capacitors L_{UC} as functions of the delay element order R are given by the following equations:

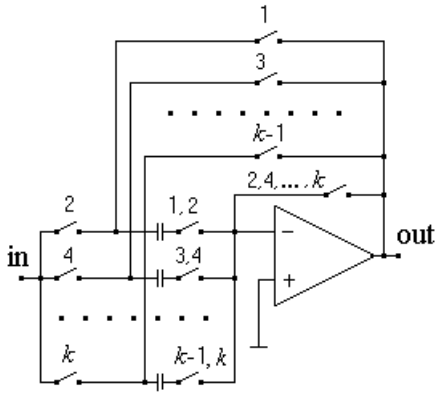


Figure 3.25: Higher order odd delay element

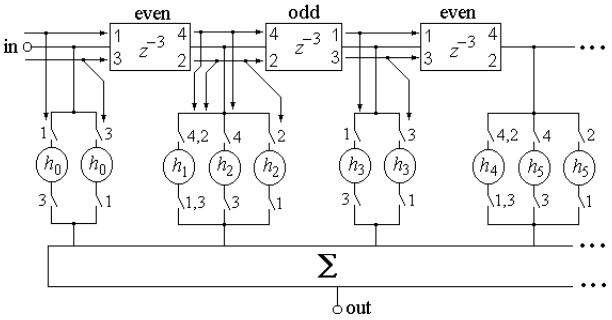


Figure 3.26: Conception of the SC FIR filter with even and odd delay elements of order $R = 1$

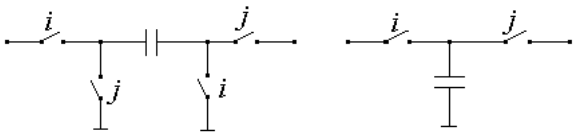
$$L_{\mathrm{S}} = 1 + 3(R+1)\,, \tag{3.25}$$

$$L_{\mathrm{UC}} = R + 1\,. \tag{3.26}$$

These values together with dimensions of UC's, S's, and OA's, which can be considered as constants for a given CMOS technology, determine the total chip area [34]. In consequence, the dimensions of the entire delay line can be precisely calculated.

3.6.2 Even-odd delay line structures

Using described above even and odd delay elements it is possible to realize tapped delay lines and entire SC FIR filters. An idea of the delay line structure with the elements of order $R = 1$ is shown in the Figure 3.26. The respective scheme is presented in the Figure 2.7. It is assumed that one clock phase corresponds to $z^{-0.5}$.



(a) (b)

Figure 3.27: Coefficient branches: (a) an inverting branch, (b) a non inverting branch

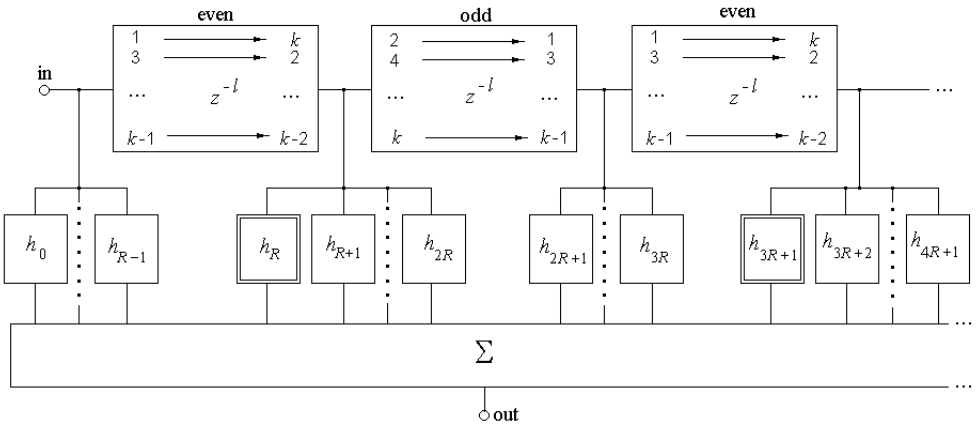


Figure 3.28: Conception of the even-odd delay line structure for $R > 1$

A single delay element realizes a transfer function of $z^{-1.5}$ (delay by 3 clock phases). Due to the alternative connection of even and odd elements, signal samples can be read along the delay line either in even or in odd clock phases. The consequence is that in order to realize filter coefficients, additional, equalizing delays are necessary. That is why at times we need two coefficient branches to realize a single filter coefficient (it is assumed that the filter output is produced in odd clock phases).

Generally, two branch types are used: an inverting branch of Figure 3.27 (a) for positive coefficients and a non inverting branch (a toggle-switched capacitor) of Figure 3.27(b) for negative coefficients [1].

Using a delay line with the higher order even and odd delay elements we can realize R+1 filter coefficients at outputs of even delay elements and R filter coefficients at outputs of odd delay elements. A block diagram of the even-odd delay line with higher order elements is presented in Figure 3.28. In the Figures 3.29 and 3.30 detailed diagrams for the filter coefficient branches are shown.

To calculate the maximum and the minimum filter order N_{MAX} and N_{MIN}, respectively, for a given number of delay elements m and for a given order R of the delay element, we can use the equations (3.27) and (3.28)

$$N_{\mathrm{MAX}} = (m+1)R + (m+1) \text{ div } 2 - 1\,, \tag{3.27}$$

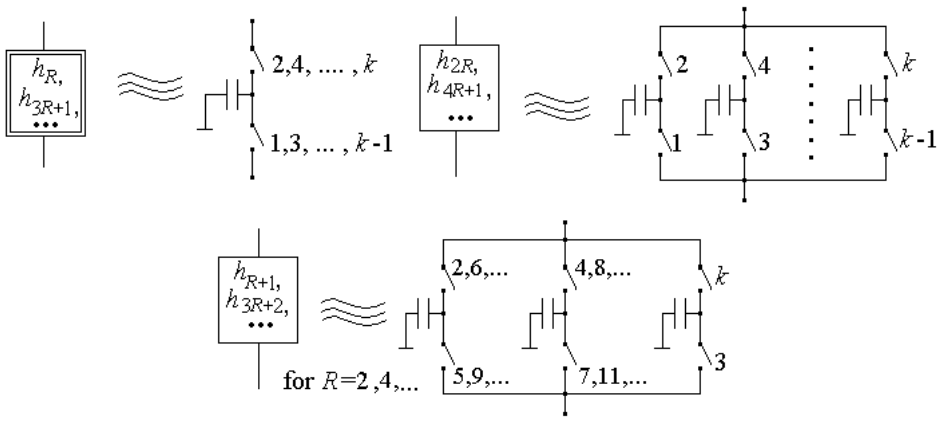


Figure 3.29: Coefficient branches at outputs of even delay elements

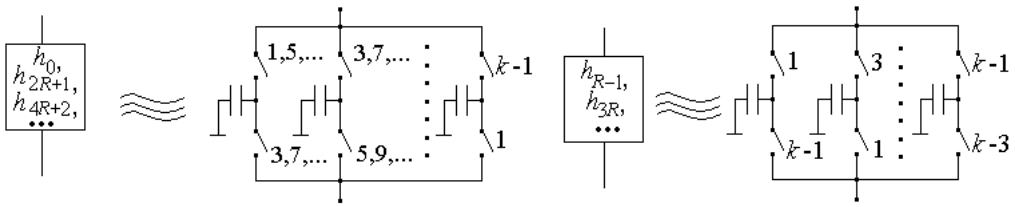


Figure 3.30: Coefficient branches at outputs of odd delay elements

$$N_{\mathrm{MIN}} = mR + m \text{ div } 2\,, \tag{3.28}$$

where "div" is the result of natural division.

For given R and m, the obtainable filter order is in the range of $N \in (N_{\mathrm{MIN}}, N_{\mathrm{MAX}})$. Generally, for a given N, the higher order R the shorter is the required delay line, i.e., the smaller is the number m. This decreases the number of active elements and consequently – the power consumption. In shorter delay lines the number of read and write operations per one signal sample along the delay line is lower. This decreases the total rewriting error and improves the filter frequency response.

The required number of coefficient branches (equal to the number of CC's) is given for the maximum order N_{MAX} by equation (3.29)

$$L_{\mathrm{CC}} = (m+1)(R+1)(R+2)/2 + (m+2) \text{ div } 2\,. \tag{3.29}$$

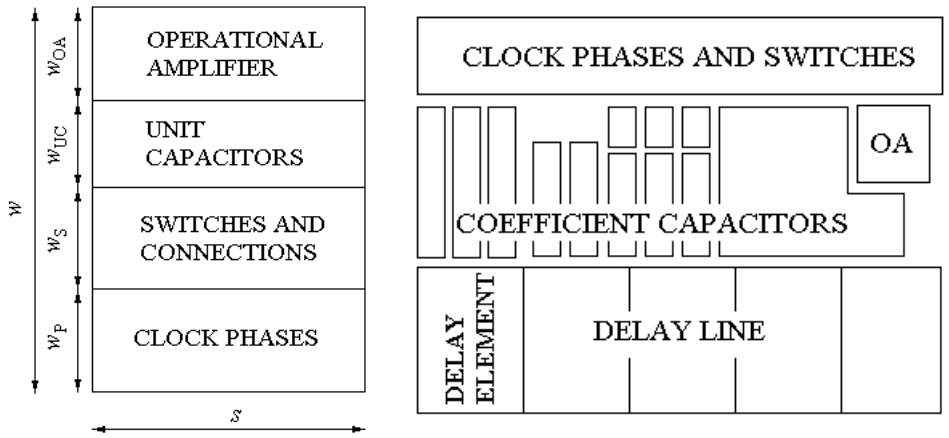


Figure 3.31: Topology of a delay element (left hand side) and of entire structure (right hand side) for the CMOS realization

3.6.3 Theoretical evaluation of the chip area of the even-odd delay line structures

The chip area is an important parameter, which directly influences the chip cost. A precise chip area estimation is not an easy task for various structures and filter responses. It depends not only on the numbers R and N but also on the values of the filter coefficients, which in the FIR SC filters are realized by the ratios of the capacitor values. That is why the chip area must be analyzed separately for different filter responses. In this section we analyze two characteristic types of frequency responses, which can be treated as two extreme cases (see also Section 3.2). The first one is a filter with equal coefficients, i.e., with zero spread of CC's. The second one is a filter with flat (Butterworth type) passband, i.e., with a very large coefficient spread (the normalized coefficients form the Pascal triangle [34, 37]).

In the first case, each CC contains only one UC. Thus the total number of the UC's realizing filter coefficients can be computed using equation (3.29). Additionally, it is necessary to add the area of the feedback capacitor (this connected to the OA output). Its area is related (e.g., equal) to the sum of areas of these CC's, which are discharged in the same clock phase. Typical topology of one delay element and also of entire structure is shown for the CMOS realization in the Figure 3.31. For the CMOS 0.8μm technology the chip area can be calculated using the equations (3.30) – (3.33)

$$P = P_{\mathrm{DEL}} + P_{\mathrm{CC}} + P_{\mathrm{SP}} + P_{\mathrm{OAW}}\,, \tag{3.30}$$

$$P_{\mathrm{DEL}} = (w_{\mathrm{P}} + w_{\mathrm{S}} + w_{\mathrm{UC}} + w_{\mathrm{OA}}) \cdot s \cdot m\,, \tag{3.31}$$

$$P_{\mathrm{SP}} = m \cdot s \cdot (w_{\mathrm{P}} + w_{\mathrm{Sout}})\,, \tag{3.32}$$

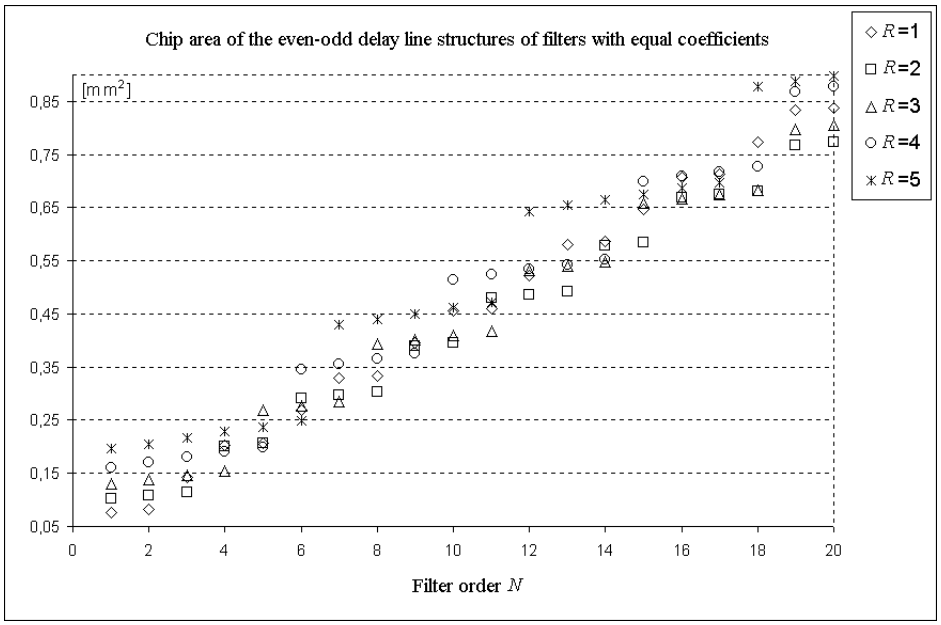


Figure 3.32: Chip area for filters with equal coefficients

$$k_1 = 4(R+1)+2\,. \tag{3.33}$$

P is the area of the entire structure, P_{DEL} is the delay line area, P_{CC} is the area of the coefficient capacitors, P_{SP} is the area of the switches and clock paths in the summer circuit, P_{OAW} is the area of the output OA. The values of variables s and w_{xx} in above equations are the estimates calculated on the basis of experience gained by the author during the design of other SC filters [34] ($w_{\mathrm{P}} = k_1 \cdot 5\,\mu$m, $w_{\mathrm{S}} = 80\,\mu$m, $w_{\mathrm{UC}} = 65\,\mu$m, $w_{\mathrm{OA}} = 70\,\mu$m, $w_{\mathrm{Sout}} = 90\,\mu$m, $s = L_{\mathrm{S}} \cdot 20\,\mu$m, $P_{\mathrm{CC}} = L_{\mathrm{CC}} \cdot 1600\,\mu\mathrm{m}^2$, $P_{\mathrm{OAW}} = 12000\,\mu\mathrm{m}^2$). Parameter k_1 is the number of the clock paths, which is higher than the number of clock phases k because particular switches are driven by more than one clock phase. In fact k_1 is the number of all combinations of the clock phases needed to drive the structure.

The chip area is presented as a function of the filter order N in the Figure 3.32 for filters with equal coefficients and in the Figure 3.33 for the Butterworth type (flat passband) filters. Figures 3.32 and 3.33 show that the chip area depends on many parameters, e.g., values of filter coefficients, filter order N, and the delay element order R. For SC FIR filters with low coefficient spread the chip area is similar for different delay element orders R. Greater differences are observable for the Butterworth type (flat passband) filters. In both cases, however, there exist filter orders, for which higher order delay elements bring some chip area savings. Generally, using the structures with higher orders R, we need smaller number of OA's. This decreases the power consumption but complicates the clock system. In consequence, for different applications we must consider different criteria in order to choose the optimal structure suitable for a given application.

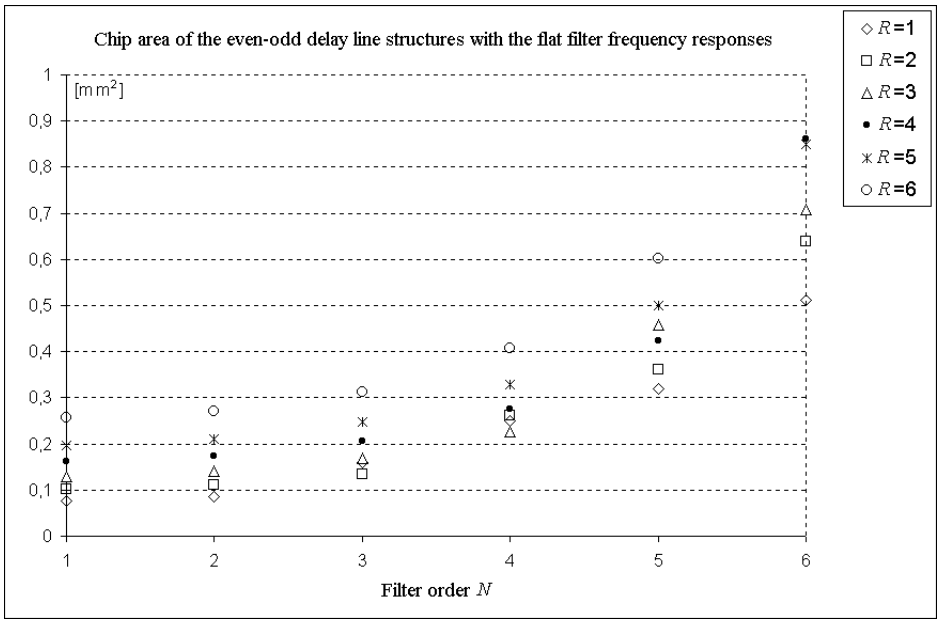


Figure 3.33: Chip area for Butterworth (flat) filters

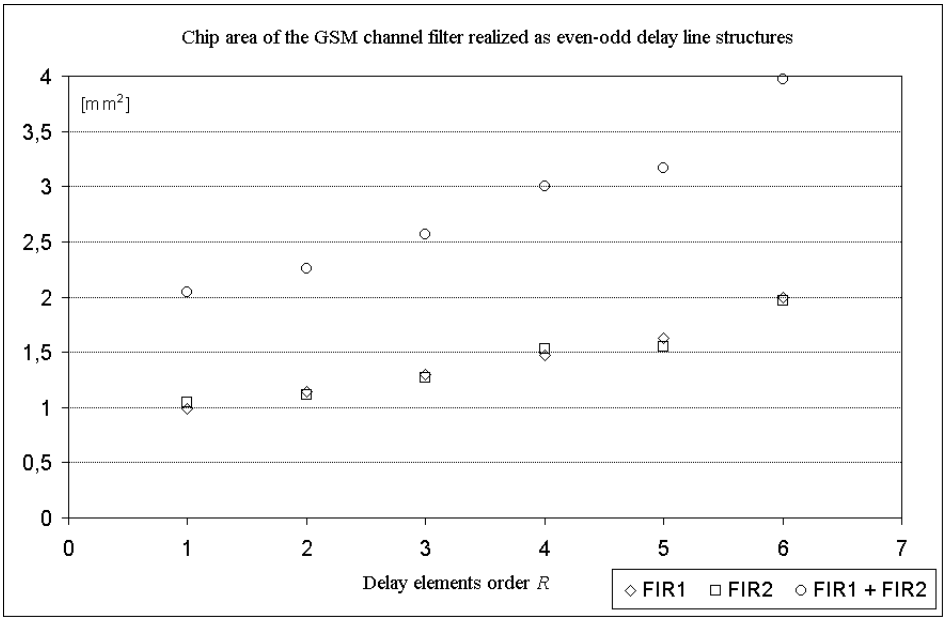


Figure 3.34: Chip area for GSM channel filter

In the next chapter the chip realization of the even-odd delay line structure is presented, in which the parameter is $R = 1$. The application of this filter is the GSM channel filter with the frequency response presented in the Figure 4.1. On the basis of the equations (3.30) – (3.33) we evaluated the chip area for the example of the GSM channel filter for different values of R parameter. The results are presented in the Figure 3.34. For $R = 1$ the result is close to the real chip area and differs by about 10% only, what is good result. It is worth noting that chip area increases moderately with the parameter R, e.g., increasing value of the R parameter to 3, the chip area will increase by only 25%, and, as a result of that, we obtain the structure with a smaller number of OA's, and with lower power consumption and better signal quality.

Chapter 4

CMOS realization of the chosen SC FIR filter structures

This Chapter is dedicated to the description of integration of chosen SC FIR filter structures for practical verification of the results presented in the last Chapter. As an application example a GSM base station channel filter was used. Its design specification is presented in the next Section.

First prototype of this filter was based on the Gillingham delay line structure (No. 3) [39, 41, 42]. This structure was first chosen because of some important advantages: small chip area and simple clock system (only two complementary clock signals) [38]. The last parameter was important as the filter was driven by an external clock system, and the number of in/out pins was rather limited.

In the second prototype an improved version of the structure No. 3 and the filter with even-odd delay elements (No. 1) were implemented for comparison [47, 51, 52]. Moreover internal clock systems, which can be used optionally to the external clock systems by a specially designed switching circuit were also implemented in the second prototype.

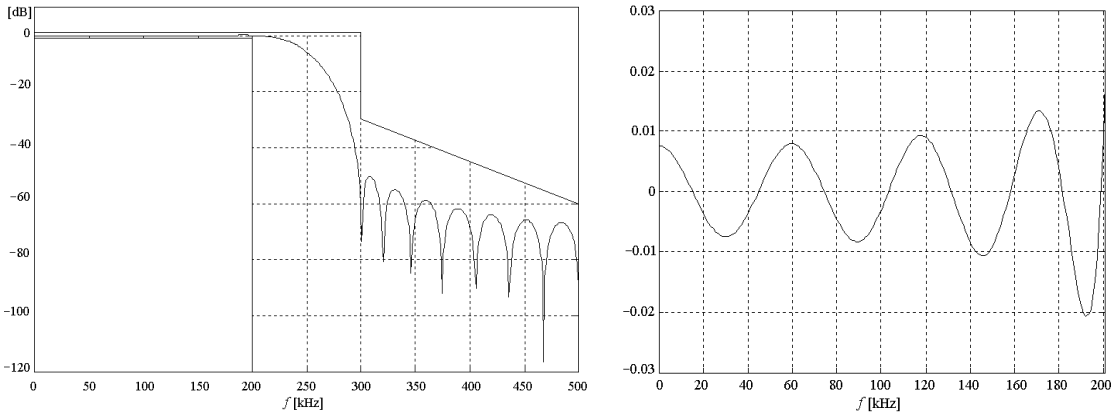
In the next Section the GSM filter specification and its partition into two optimized sections is presented. These results were published by A. Dabrowski and D. Cetnarowicz in [40]. In this dissertation their results are partially presented, because they are necessary for the next stages of the presented design process.

In Section 4.2 we design the building blocks of the SC FIR filters: operational amplifiers, capacitors, switches. Next in Section 4.3 the design of the clock systems, both external and internal, is presented. The last two Sections 4.4 and 4.5 are dedicated to the design of the Gillingham and the even-odd delay line structures. In these Sections the measurement results of the prototypes are also shown.

4.1 Specification of the GSM channel filter

For verification of the design methods presented in previous Chapters the test application has been chosen, namely the channel filter, which works in the base band in GSM receivers [54]. Design specifications for this filter are presented in Figure 4.1a. The upper signal frequency range is equal to 500 kHz.

The chosen attenuation curve, which meets all requirements, is presented in Figure 4.1a, with the passband part depicted in Figure 4.1b. This is just the frequency response of an FIR filter of order 31, designed with the Kaiser window with the parameter β=4.6017. As can be seen in Figure 4.1, the required specifications are safely fulfilled with this filter. Furthermore, its frequency response is nearly optimal, because it fulfils the given requirements with a margin, which is almost uniformly distributed. This solution is assumed as the ideal transfer function for the considered SC GSM channel filter, which is to be designed. Ideal values of the filter coefficients are listed in the second column h_i of Table 4.1.



(a) (b)

Figure 4.1: Specifications for the GSM channel filter [40]: (a) frequency response of the filter designed using Kaiser window, (b) passband part of the frequency response

Values of SC FIR filter coefficients are ratios of two capacities: a coefficient capacity (that at the input of the summer circuit) divided by a capacity of the OA feedback capacitor [1]. The latter capacity is the common denominator for all coefficients:

$$h(k) \cong \frac{C_k}{C}\,. \tag{4.1}$$

Manufacturing of SC integrated circuits is associated with a limited accuracy of the capacitors (the problem was theoretically analyzed by Mitra in [18]). Capacitors are realized as multiples of small unit capacitors (UC's) connected in parallel [1, 41]. Thus SC FIR filter coefficients are quotients of two integers and should be optimized by discrete optimization techniques.

The bigger the number of unit capacitors forming coefficient capacitors the smaller are coefficient errors. Due to this fact, unit capacitors should be as small as possible (their number simultaneously increases). However, the smallest realizable unit capacitor values are limited by a given CMOS technology. Additional problem concerns parasitic capacities, which in the case of small UC's, have a considerable effect on the frequency response. Another technological and economical limit is the maximum acceptable chip area, of which the total capacitor area [34, 37] is a substantial part. Due to this fact UC's cannot to be too big.

Exact values of the filter coefficients must be approximated by ratios of integers. In practice a coefficient with the smallest absolute value must be selected first. If we search for the minimal chip area of all coefficient capacitors, the value of this coefficient is normalized to one, i.e., realized as a single UC. In Table 4.1 there are two coefficients with the smallest absolute value $h(1) = h(32) \cong -0.000759437$. Computing the inverse and approximating it by an integer we get the number $c = 1317$, which is the smallest possible candidate for the common denominator of all coefficients. However, instead of directly using this value as the denominator, it was optimized in [40] by minimizing the sum of squares of all coefficient errors and by minimizing the sum of squares of the sampled passband attenuation errors. In both cases the optimum value is $c = 1318$, which is very close to 1317. Other filter coefficients were calculated by multiplying their real values by this factor. Coefficient values normalized in this way were rounded to integer numbers. The rounded values are listed in Table 4.1. The corresponding relative coefficient errors are listed in the column named "Error". Absolute values of these errors vary from 0.01% up to 5.09%. Although Table 4.1 contains optimized coefficients, their final evaluation can only be made on the basis of the examination of the resulting filter frequency response shown in Figure 4.2.

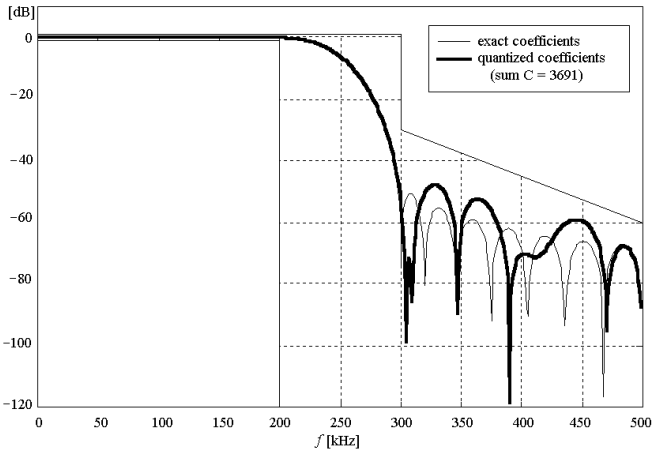


Figure 4.2: Frequency response of the direct realization of the 31'th order SC FIR filter according to coefficient values in Table 4.1 [40]

The results achieved are sufficient in both the passband and the stopband. However, the resulting total amount of capacitors equals 3688 UC's (the coefficient spread is equal to 592) which is about 6 mm^2. This number is far from the optimal and in the

Table 4.1: Filter coefficients: real, rounded and error [40]

i	h_i	Rounded coefficients	Error [%]
1	-0.000759437	-1/1318	0.09
2	-0.00144393	-2/1318	-5.09
3	0.00239717	3/1318	5.05
4	0.00367784	5/1318	-3.15
5	-0.0053547	-7/1318	0.81
6	-0.00751148	-10/1318	-1.01
7	0.0102554	14/1318	-3.58
8	0.0137331	18/1318	0.55
9	-0.0181589	-24/1318	-0.28
10	-0.023872	-31/1318	1.47
11	0.0314544	41/1318	1.10
12	0.0420089	55/1318	0.66
13	-0.0579115	-76/1318	0.43
14	-0.0853702	-112/1318	0.46
15	0.147218	194/1318	0.02
16	0.449207	592/1318	0.01
17	0.449207	592/1318	0.01
18	0.147218	194/1318	0.02
19	-0.0853702	-112/1318	0.46
20	-0.0579115	-76/1318	0.43
21	0.0420089	55/1318	0.66
22	0.0314544	41/1318	1.10
23	-0.023872	-31/1318	1.47
24	-0.0181589	-24/1318	-0.28
25	0.0137331	18/1318	0.55
26	0.0102554	14/1318	-3.58
27	-0.00751148	-10/1318	-1.01
28	-0.0053547	-7/1318	0.81
29	0.00367784	5/1318	-3.15
30	0.00239717	3/1318	5.05
31	-0.00144393	-2/1318	-5.09
32	-0.000759437	-1/1318	0.09

next subsection it is shown that it can be substantially reduced by factorizing the filter transfer function into a number of partial functions and by cascading the corresponding filter sections [37, 40]. In the extreme case the transfer function may be decomposed into first-order factors given by equation (4.2)

$$H(z) = \sum_{k=1}^{N+1} h(k) z^{-k+1} = h(1) \prod_{k=1}^{N} (1 - \alpha_k z^{-1}) , \tag{4.2}$$

where α_k for $k = 1, ..., N$ are zeros of $H(z)$. If $H(z)$ is a real function, the complex zeros occur in conjugate pairs and may be combined to form second-order sections with real coefficients [37]. Thus for even N we have the equation (4.3)

$$H(z) = h(1) \prod_{k=1}^{N/2} [1 + b_k(1) z^{-1} + b_k(2) z^{-2}] . \tag{4.3}$$

According to equation (4.3), transfer function $H(z)$ may be realized as a cascade connection of second-order FIR sections (with exception for a unique first order or third order section in case of odd N).

Zeros of transfer function $H(z)$ were computed using MATLAB environment in [16, 40]: there are 5 real zeros and 13 complex conjugated pairs. As a result, the considered filter can be realized as a cascade of maximum 18 partial filters. These 18 sections form building blocks present in a cascade realization of the considered filter. In this case coefficient spread in particular building blocks is much smaller than this observed in the direct, realization (considered previously). In consequence, using the same discrete optimization method for coefficients, the total area of capacitors can be drastically reduced in the cascade realization – in our case down to about 90 UC's (i.e., 0.15 mm^2). However, this procedure does not guarantee that the resulting frequency response is acceptable. In fact, the response obtained by this means (plotted in Figure 4.3) is far from being acceptable. This results from the fact, that the rounding of the filter coefficients introduces in every section an error. Since the resultant transfer function of all sections connected in series is equal to the product of particular transfer functions, the errors cumulate and the total error can be much bigger than in the case of the direct realization.

From Figure 4.3 we conclude that it is necessary to increase the accuracy of the coefficient approximation. This can be achieved by multiplying the numerator and the denominator of the quotient in expression (4.1) by a choosen factor m_x. Frequency responses corresponding to approximations of this kind are also shown in Figure 4.3. Factors m_x chosen for testing are equal to 10, 15, and 30. Starting with $m_x = 15$ the frequency response fulfils the required specifications but in order to guarantee some safety margin in the passband and in the stopband, the factor m_x should be about 30. The cost of this procedure is an increase of the total area of capacitors by, roughly speaking, this same factor. The overall capacitor area is represented by sum C in Figure 4.3. For $m_x = 30$ the total area is 3168 UC's. In result, the cascade filter realizations

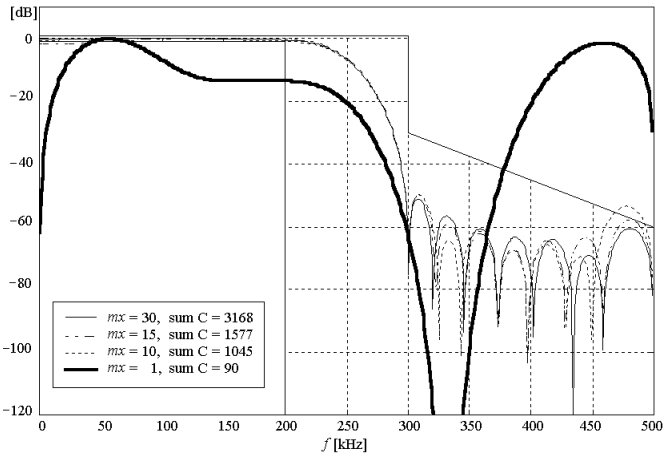


Figure 4.3: Unacceptable frequency response of cascade realization with coarse coefficients [40]

Table 4.2: Final filter coefficients [40]

i	First section	Second section
1	2	1
2	7	-1
3	9	-1
4	10	2
5	17	4
6	15	-2
7	-5	-9
8	-17	-1
9	-5	11
10	11	11
11	7	-4
12	-5	-19
13	-4	-19
14	2	-14
15	1	-9
16	-1	-7
17		-2
Total	54	47

with the maximum number of sections (building blocks) do not bring any profit [40]. This means that the total area of capacitors remains approximately the same as in the direct structure, which was presented and discussed in previous Section.

The realizations of the filter presented above are two extreme cases. In practice such a filter can by realized by different combinations of sections of order higher than 2. Checking all possible combinations is a quite complicated computational task. Be-

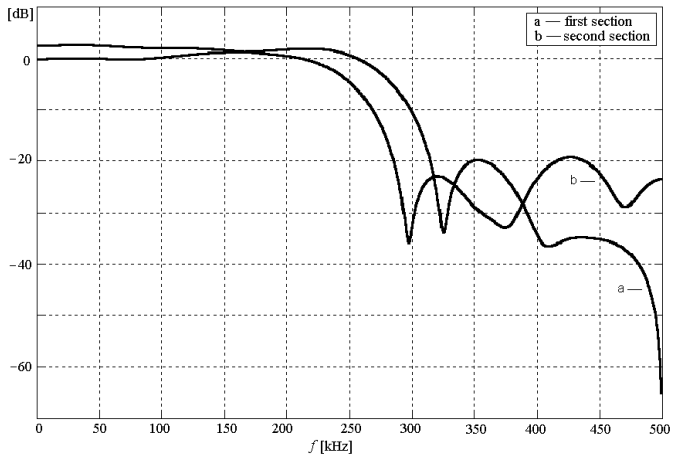


Figure 4.4: Frequency responses of individual filters in the final cascade realization [40]

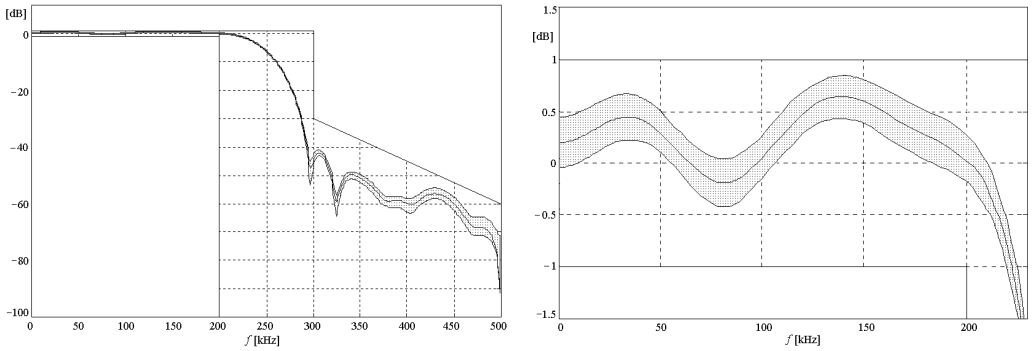


Figure 4.5: Frequency response of the final filter realization [40] with the area of estimated deviation due to sensitivity: (a) the whole curve, (b) the passband part

cause of this, realization with only two sections was checked [40]. In this case the number of configurations to check was reduced to 24310. In order to find the optimum decomposition the complete search among all these possibilities was made. In parallel, optimizations were also performed using the genetic approach, which needed by two orders of magnitude less searches. Genetic computations led to the satisfactory result being very close to the optimum configuration.

Values of the final filter coefficients are listed in Table 4.2. Frequency responses of both sections are plotted in Figure 4.4. The resultant frequency response is shown in Figure 4.2. As it can be seen in Figure 4.2, the obtained frequency response fulfils the required specifications with a sufficient safety margin. It should be stressed that the total area of capacitors is 336 UC's only (i.e., 0.53 mm^2). This area is more than ten times less than that required for the direct realization.

Sensitivity Analysis

The implementation of capacitors in the integrated circuit is associated with errors. These errors are results of various causes [41]. On the layout stage the errors can be omitted by precise design. The errors can result from the parasitic capacities of the internal connections (it is not always possible to avoid them), of the technological process, during which in the structures occur different nonidealities especially not regular border of the capacitors etc., but these errors often can be neglected (as they are less than 1%). Because of this fact the last simulations were devoted to the analysis of sensitivity of the frequency response to deviations of coefficients [40]. It was assumed that each coefficient could be implemented with accuracy of 1%. In order to simplify the simulations it was assumed that each coefficient could have three values only: a nominal value and the values equal to $\pm 1\%$ of the nominal value. Simulation of all possible cases $3^{31} = 6.2e^{14}$ would be extremely time-consuming. That is why a simplified worst case analysis was made. It showed that the frequency response might be deviated at maximum of ± 4 dB. This is illustrated in Figure 4.5 as the gray area surrounding the frequency response computed with nominal coefficient values.

4.2 Building blocks of SC FIR filters

4.2.1 Operational amplifiers

Operational amplifiers are main building blocks of SC FIR filters. These elements are of great importance for many crucial parameters of SC FIR filters, such as the power consumption, the upper frequency range, quality of the signal (c.f., Section 3.5) and the chip area. An idea used for the design of the GSM channel filter was a possibly simple structure of the operational amplifier to minimize the chip area, as it is one of the most important requirements. On the other hand the required OA should have sufficiently perfect parameters like minimal offset voltage. It should be quick enough to recharge the summer capacitors during the required instants. Taking many conflicting criteria into account, Miller's OA shown in Figure 4.6 was chosen. This structure was used in the first prototype of the GSM channel filter as well as in the improved version in the second prototype. The Miller's OA posses many disadvantages, but is relatively simple and requires a small chip area. The HSPICE simulations and further measurements show that important parameters like the dynamic range, DC gain, gain-bandwidth (GB) product, power consumption, bias voltage, sensitivity to the supply voltage mismatch, etc. are acceptable for the presented projects [1, 44, 45].

Starting version of the Miller's operational amplifier

First version of the implemented Miller's OA is shown in Figure 4.6. One of disadvantages of this circuit is its high sensitivity to the bias voltage V_{B}. This voltage polarizes the differential pair and the MN1 transistor, which is the dynamic load of the output

transistor MP1. Influence of the voltage V_B depends on the signal frequency, as is illustrated in Figure 4.7a, b. Simulation experiments shown in these Figures were made in an inverter (inverting amplifier with gain equal to -1) configuration driven with the sinusoidal input voltage with amplitude 1 V and two frequencies: 10 kHz and 1 MHz. The bias voltage V_B changed in the range of +2.5 V to – 2.5 V. The processed signal (output voltage) was correct for V_B in the range of 1.5 V to –1.5 V (for the signal frequency of 10 kHz) and in the range of 1 V to –1.3 V (for the signal frequency of 1 MHz). The optimal value of the bias voltage is obviously close to the lowest possible value, because in this case we achieve the lowest power consumption. To show this fact, the OA supply current (I_{DD}) is also illustrated in these diagrams. This current changes in the range of 8.5 mA (the real measured value was about 0.9 mA, i.e., very close) to approximately 0. The simulations show that for higher amplitudes of the input signal, the bias voltage should be somehow higher. In consequence, the real supply current will also be somehow higher and equal to about 1–1.5 mA.

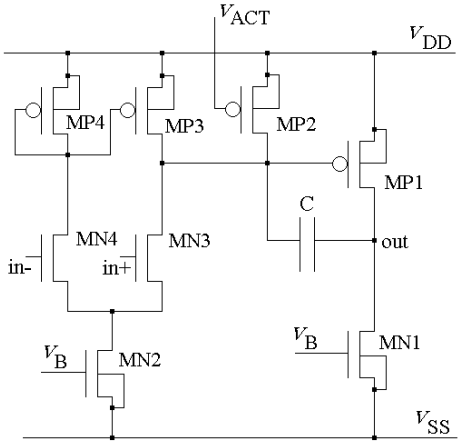


Figure 4.6: Miller's operational amplifier

The output stage of the Miller's OA works in A–class with the active load. In the OA optimized for the low power consumption, the output voltage is not symmetric, if the load is near to the output impedance, as is illustrated in Figure 4.8. Simulations were made in an inverting amplifier with gain equal to -2. The circuit was driven with a sinusoidal input voltage of amplitude 1 V and frequency 2 kHz and was loaded with resistance equal to 450 Ω. For negative voltages, if the channel width of the MP1 transistor is low (c.f., Figure 4.6), the transistor MN1 in the dynamic load is opened. When the polarization current is low, than the efficiency of the NM1 transistor is insufficient. The dashed line in the upper part of the diagram in Figure 4.8 illustrates the supply current I_{DD}.

Figure 4.9 illustrates supply currents I_{DD} and I_{SS} for the open loop operation of the OA. The dashed line illustrates I_{DD} and the thick line illustrates I_{SS}. If the output voltage is close to V_{SS}, the absolute values of both currents are equal to about 0.1 mA, but if the output voltage is close to V_{DD}, then the currents are stronger than 1.1 mA (i.e., more than 10 times stronger). The offset voltage is equal to about -5 mV. Because the

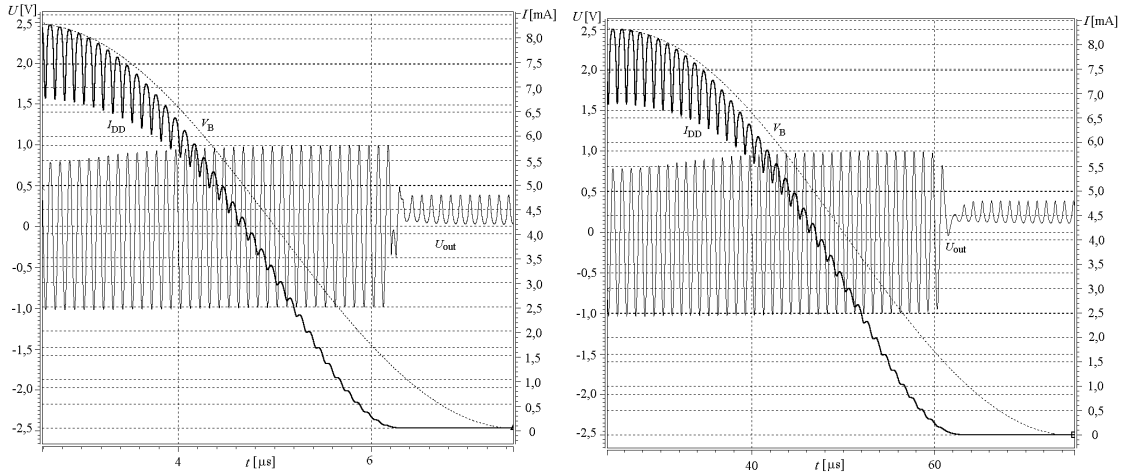


Figure 4.7: Influence of the bias voltage in the Miller's OA on the output voltage and the I_{DD} current for the input signal frequency: (a) 10 kHz, (b) 1 MHz

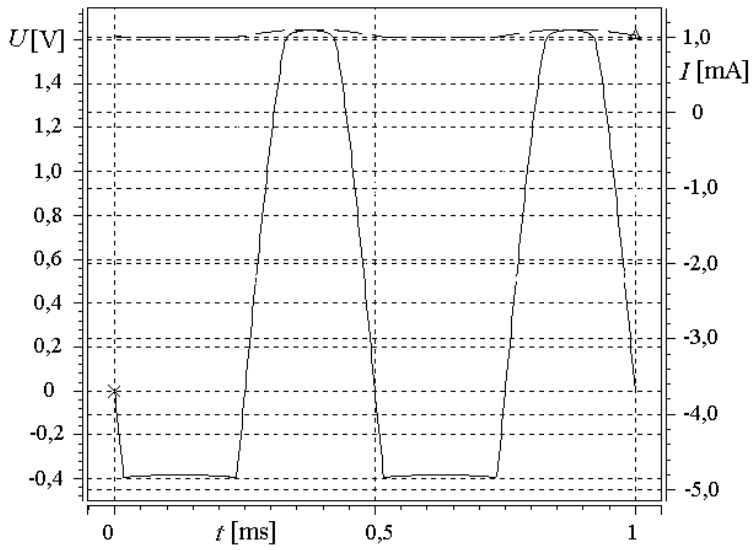


Figure 4.8: The OA's output voltage with the resistance load equal to 450 Ω

channel filter is driven by the 1 MHz clock signal, the OA must have good parameters at this frequency. Figure 4.10 illustrates the frequency response and the phase response of the OA in the open loop configuration.

The GB product of the presented OA is equal to 2.88 MHz, and the DC gain is higher than 80 dB [41]. These parameters strongly depend on the bias voltage V_{B}.

Layout of the analyzed version of the Miller's OA is presented in Figure 4.35. However, all above considerations show that optimization of the presented OA is necessary, first of all, by optimization of its output stage.

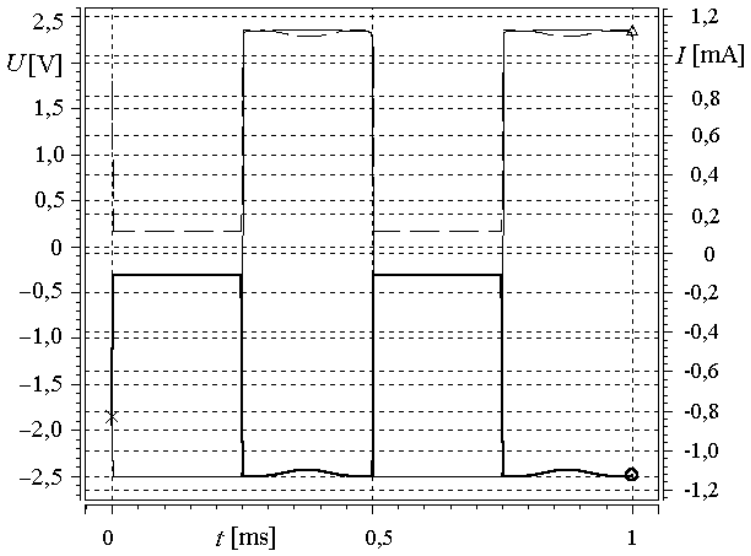


Figure 4.9: Current supply in the open loop configuration

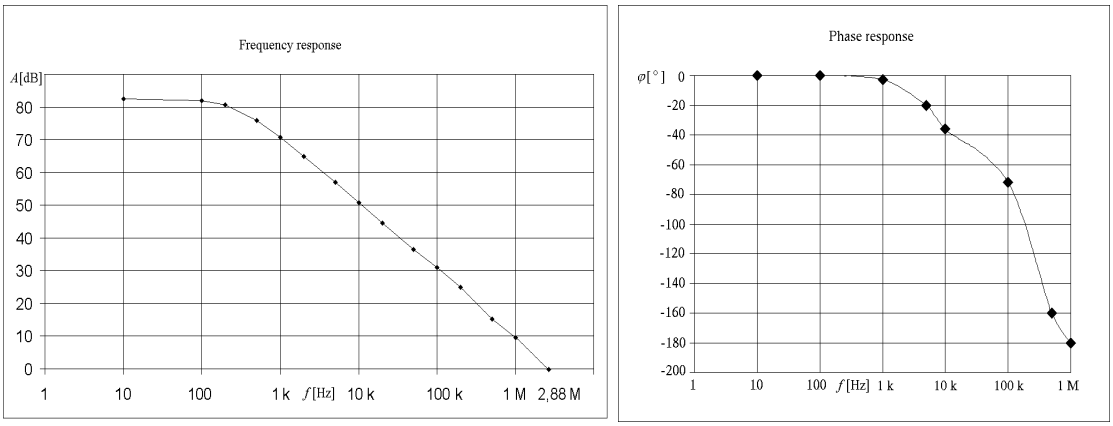


Figure 4.10: Frequency and phase response of the OA in the open loop configuration

Improved version of the Miller's operational amplifier

On the basis of experiences gained with the use of the Miller's OA presented in Figure 4.6, in the second prototype of the realized filter improved OA's were used, optimized for SC FIR integrated filters. Modifications concern the output OA stage. Instead of the A–class output amplifier with the dynamic load, complementary AB-class amplifier was designed. The corresponding circuit is shown in Figure 4.14. Additionally, the MP2 transistor (driven with the voltage V_{ACT}) was removed. This transistor was used only to switch off the output stage.

In the improved version of the OA an important issue is the proper choice of the MP1 and MN1 transistor dimensions (the width and length of the channel). Experiences show that the optimal ratio of channel widths between the MP1 and MN1 transistors

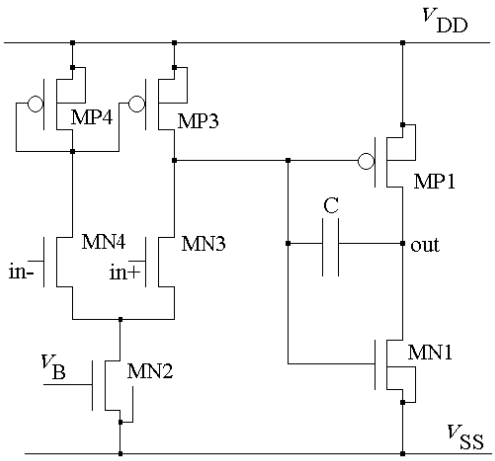


Figure 4.11: Improved version of Miller's OA

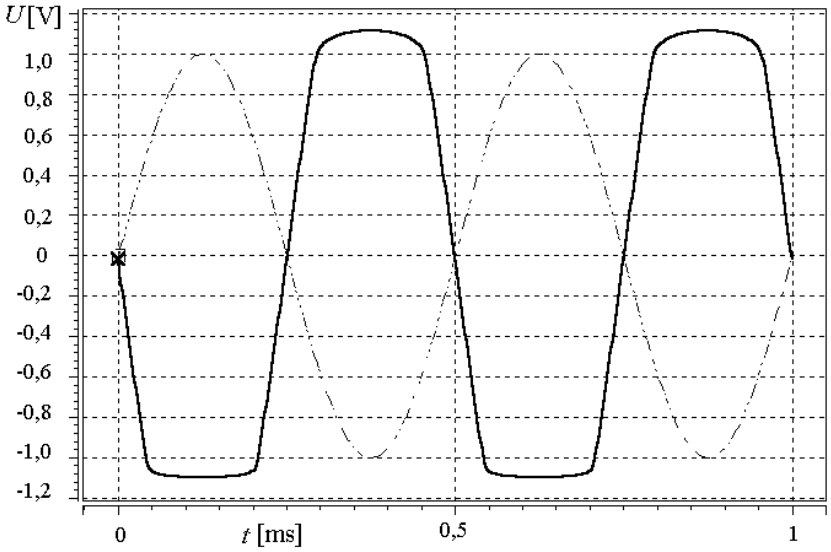


Figure 4.12: Output voltage for resistive load equal to 1 kΩ

is as 3:1. Increasing of the channel width or decreasing of the channel length increases the output current and decreases the value of the output impedance. The transistor dimensions influence also the GB product. After optimization the achieved value of this parameter is equal to 11.5 MHz. The value of the output impedance is equal to 850 Ω. In this case the minimum value of the current I_{DD} is equal to 0.65 mA. Values of the transistor dimensions chosen after the optimization process are in fact compromise values. Finally, the channel lengths of both transistors MP1 and MN1 are equal to 1 μm, and the channel widths are equal to 15 μm and 5 μm, respectively.

The offset voltage is in this case equal to -17 mV. The minimum value of the load resistance, which does not distort the output signal (with amplitude 2 V), is equal to

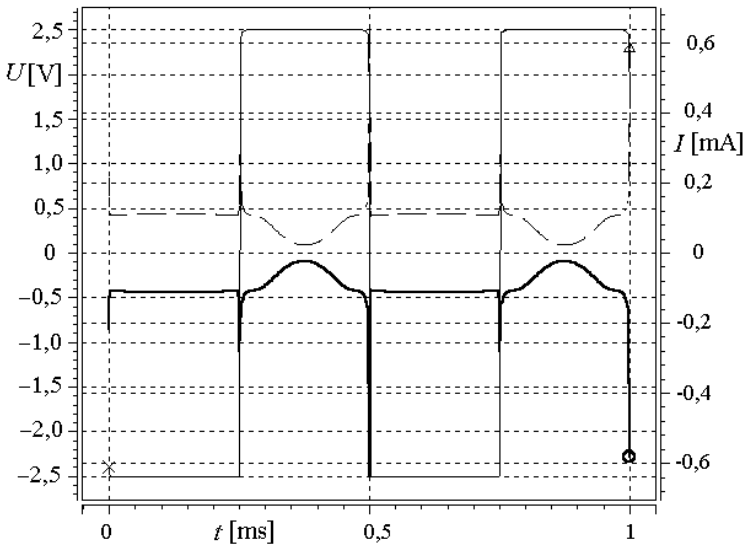


Figure 4.13: Supply currents in the open loop configuration

5 kΩ in comparison with 4 kΩ for the structure presented in Figure 4.6. Although the minimum output load's value is higher than in the first version, this is not critical, because loads of the OA are greater than this minimum value and the improved OA works symmetrically also for loads with values close to the output impedance (compare Figure 4.12 with Figure 4.8).

The HSPICE netlist of the improved version of the Miller's OA containing all transistor dimensions is presented below:

```
MP3 WE2 WE1 VDD VDD MODP L=3.00000010611257E-6 W=31.2000011035707E-6
MP4 WE1 WE1 VDD VDD MODP L=3.00000010611257E-6 W=31.2000011035707E-6
MP1 OUT WE2 VDD VDD MODP L=1.0000009348878E-6 W=15E-6
MN2 VSS VB WE3 VSS MODN L=3.00000010611257E-6 W=18.5999997484032E-6
MN3 WE2 INPLUS WE3 VSS MODN L=3.00000010611257E-6 W=21.6000007640105E-6
MN4 WE1 INMINUS WE3 VSS MODN L=3.00000010611257E-6 W=21.6000007640105E-6
MN1 VSS WE2 OUT VSS MODN L=1.0000009348878E-6 W=5E-6
```

Figure 4.13 (compare with Figure 4.9) illustrates time waveforms of the supply currents in the improved version of the Miller's OA in the open loop configuration. It can be seen that the absolute value of both currents is equal to about 0.1 mA and this value is almost independent of the output voltage. During the switching moments only the absolute value of the currents increases to about 0.6 mA.

Parameters of the improved OA are less sensitive to the bias voltage V_{B}, than those of the previous structure (compare Figure 4.14 with Figure 4.7). For the bias voltage V_{B} equal to –1.0 V, OA consumes a current equal to 0.65 mA. The lowest V_{B}, which allows the OA to work properly is equal to -1.9 V. In this case I_{DD} is equal to about 0.53 mA.

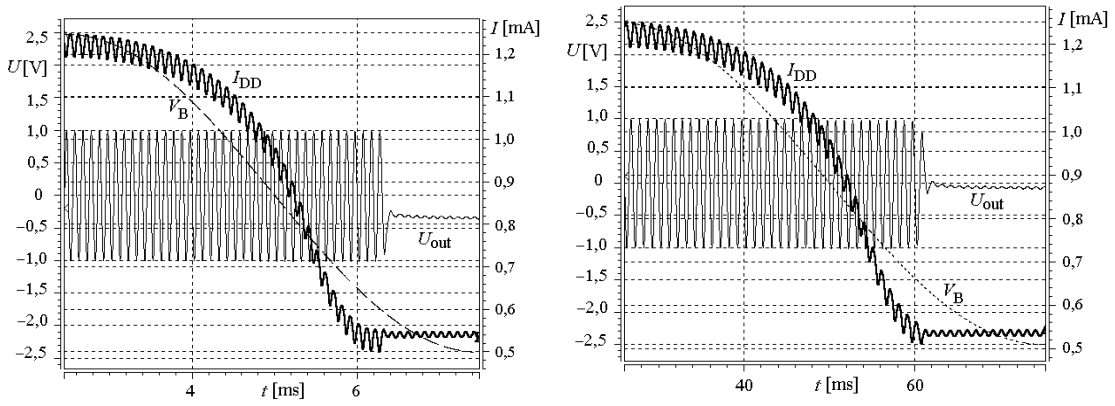


Figure 4.14: Influence of the bias voltage in the improved version of the Miller's OA on the output voltage and the supply current for the input voltage of frequency: (a) 10 kHz, (b) 1 MHz

4.2.2 Capacitors and switches

Proper realization of the coefficient capacitors (CC's) is a very important task, because values of these capacitors directly influence the filter characteristics. CC's must be realized with great precision. They are therefore made as parallel connections of unit capacitors (UC's). This allows to preserve equal area-to-perimeter ratios in capacitors of different values. In consequence, influence of the edge parasitic capacity is the same for all capacitors. To secure the full symmetry of all UC's, it is necessary to add some dummy unit capacitors around the real UC's realizing particular CC's. In this way all unit capacitors are surrounded on all sides by other unit capacitors and work in identical conditions. Both plates of dummy capacitors are connected to the highest voltage (V_{DD}). This technique is accurate enough, because in SC circuits we are interested in exact capacity ratios rather than in exact absolute capacitor values. Also, from the perspective of the manufacturing process, dummy capacitors are of great importance. They allow us to preserve the uniformity in etching of layers. The layout realization of the coefficient capacitors is presented in Figure 4.33.

Switches are realized as parallel connections of the NMOS an PMOS transistors. The important parameters here are the dimensions of the transistors. To minimize the on-resistance, the channel width should be high, but then the area of such elements will also be high. On the other hand we must remember that in SC filters the charge between capacitors flows through the channels of the transistors in switches. If the resistance of the transistors is high, then the time constants of recharging the capacitors will also be high and the maximum frequency range will be reduced. Figure 4.15 shows filter output signal in the case of incorrect dimensions of the transistors in the switch. On-resistance of the switch (and the resultant time constant) must be low enough to enable full discharging of the capacitors. Figure 4.16 shows a situation, in which transistor channel width is increased as compared to Figure 4.15.

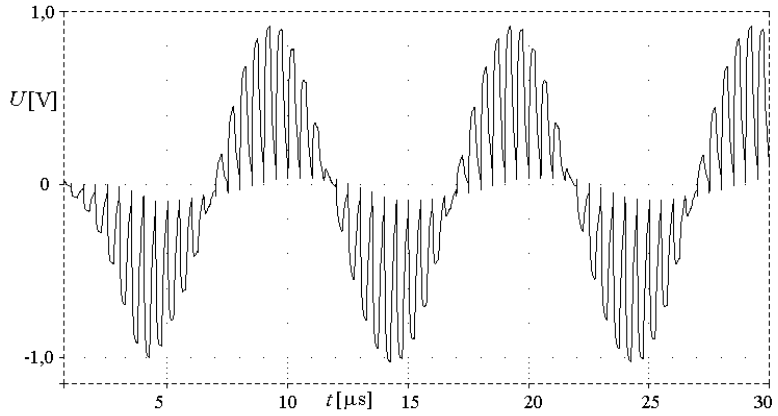


Figure 4.15: Output signal in the case of incorrect dimensions of transistors in the switch

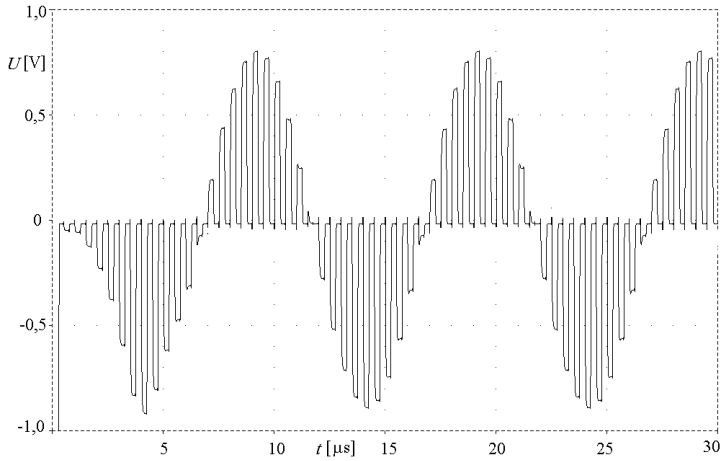


Figure 4.16: Output signal in the case of proper dimensions of transistors in the switch

4.3 Control clock systems

Among parameters of SC FIR filter structures one the most important is the complexity of the required clock systems [38, 43, 49]. Inaccurate clock can substantially reduce the filter performance and the chip complexity.

Clock systems can be quite different for various SC FIR filter structures. For some of them only a simple two-phase clock is needed, while for the others a very complicated multiphase clock is necessary. In Section 3.3 theoretical assessment of the clock systems for particular SC FIR filter structures is presented. Solutions presented there became the basis for the practical realizations of the clock systems presented in this Subsection.

In Sections 4.4 and 4.5 we present realization of the experimental integrated circuits with two kinds of SC FIR structures: the delay line structure with Gillingham delay elements [35] and the delay line structure with the even-odd delay elements [46]. These filters were designed to make it possible to drive them as well by external as by internal clock systems. Switching between them is realized with a commutation unit. The circuit of a single phase commutation switch is shown in Figure 4.17. Signals S1, S2, S3, and S4 can change the system configuration as: (1) an internal clock connected to a filter (measuring of the clock under the load is possible simultaneously), (2) filter driven by external clock (internal clock disconnected), (3) internal clock measured without the load and the filter disconnected). The corresponding layout of the commutation unit is shown in Figure 4.18.

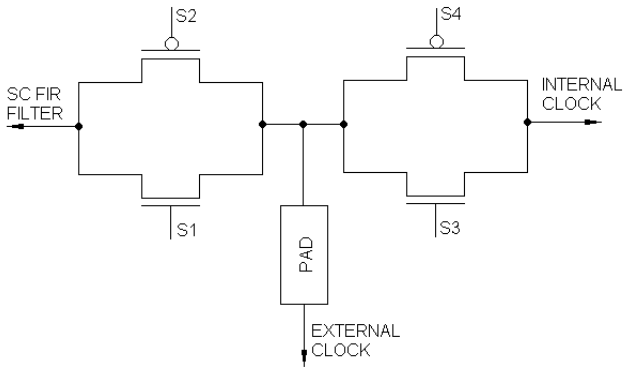


Figure 4.17: Electrical diagram of the commutation switch

Designing of both external and internal clock systems makes it possible to evaluate and compare both solutions, as each of them has advantages and disadvantages.

Internal clock systems are convenient but they consume parts of the chip area. Moreover, it is not possible to change their parameters (e.g., rise and fall or death times, delays between clock phases, etc.).

External clock systems are free of those disadvantages but require a great number of additional pins and need additional circuitry. If miniaturization of the whole device is one of the goals, the number of external elements is one of the optimization criteria. In this case an internal clock is very useful. Problems of this kind are described and evaluated in the next Subsection.

Theoretical evaluation of the clock systems for particular SC FIR filters is presented in Section 3.3. The realization of internal clock systems is presented in the next Subsection 4.3.1. Subsection 4.3.2 is dedicated to the realization of the external clock systems.

4.3.1 Internal clock systems

Internal clock systems postulated here are designed on the basis of D type flip-flops, NAND and NOT logic gates. A self-correcting synchronous counter with sixth stages

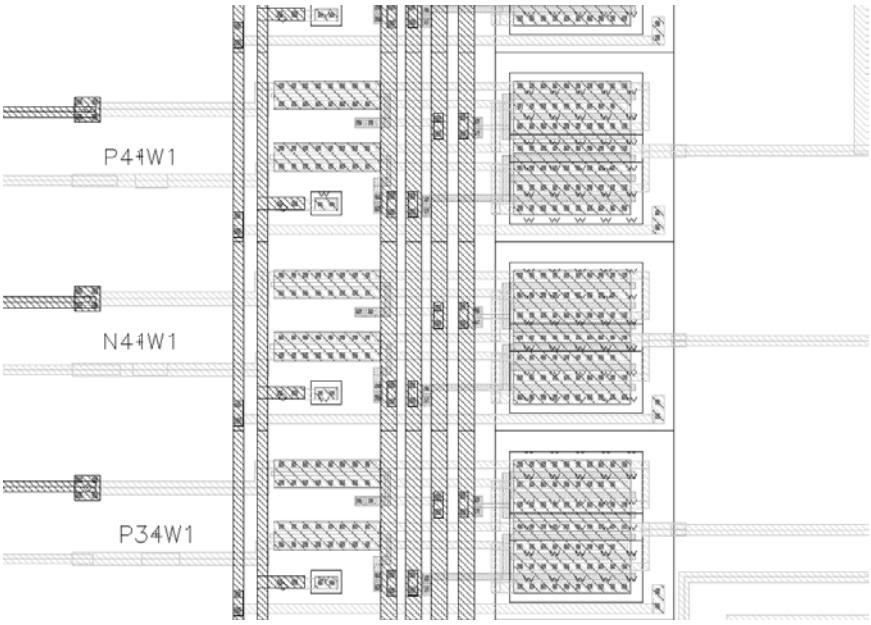


Figure 4.18: Layout of the commutation unit

(Figure 4.19) is a simple structure [12, 13], but the design process of such a system is not easy, as SC FIR filters (especially the even-odd delay line structures) are sensitive to the shape of clock impulses. Thus the transistor dimensions of logic elements have to be selected very carefully to obtain appropriate clock waveforms (c.f., Figure 3.13). As mentioned in Section 3.3, the number of physical clock signals is twice as great as the number of logical clock phases (the total number of phases and their combinations) as each clock phase controls two types of transistors. These signals are complementary, so we need only one inverter for each phase to produce all necessary signals. Silicon implementation of this idea is, however, not simple. An inverter delays the signal, and as a result of this, both transistors in the switch are opened in somehow different times. This degrades to a certain degree signals in the delay line and, consequently, the filter performance.

A proper shape of the clock impulses is a very important parameter. Complementary clock impulses must cross near to 1.5 V for voltage supply 0–3.0 V or near to 2.5 V for voltage supply 0-5 V,

thus the processed signal oscillates around 1.5 V or 2.5 V. A situation of proper crossing of the two clock impulses for NMOS transistors is shown in Figure 4.20. In Figure 4.21 an improper situation is illustrated, in which shortcuts occur (there exist short whiles, when all switches are on). This causes the loss of charge stored in the capacitors along the delay line and leads to errors. In consequence the signal along the delay line is distorted as is illustrated in Figure 4.22. In consequence the frequency response of the filter is also distorted, especially in the stopband.

In order to save the chip area and to minimize costs, the clock system should be as simple as possible. However, the simplest structures like, e.g., the asynchronous counter

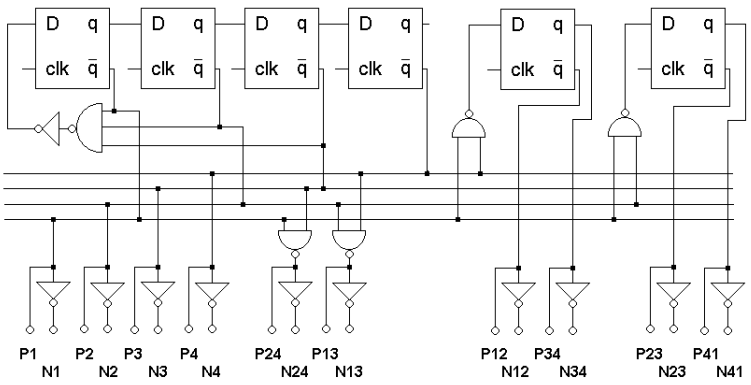


Figure 4.19: Electrical diagram of the clock for even-odd delay line structures

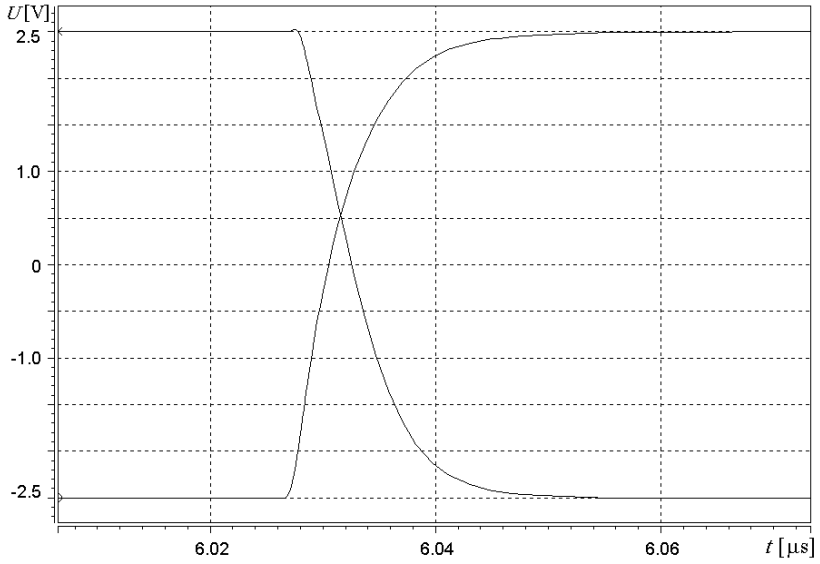


Figure 4.20: Acceptable crossing of phases 3 and 4 of clock signals generated by an internal clock

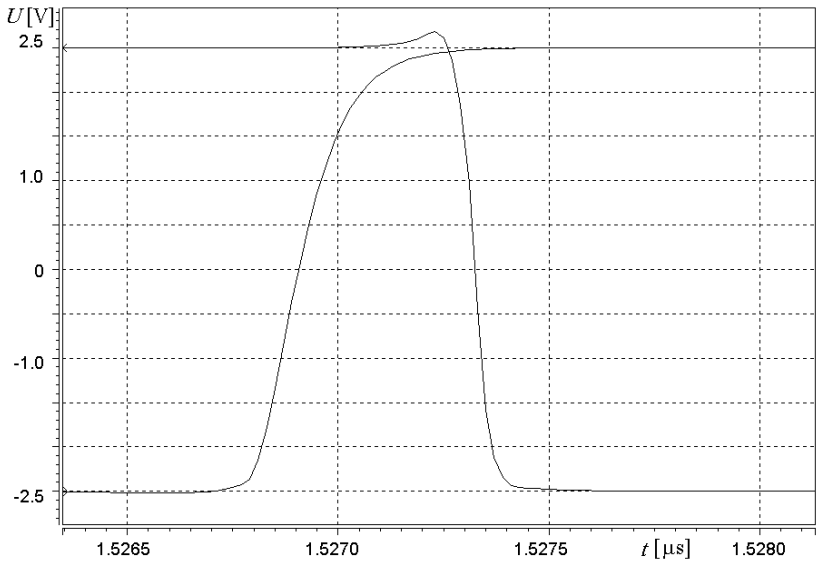


Figure 4.21: Unacceptable crossing of phases 3 and 4 of clock signals generated by an internal clock

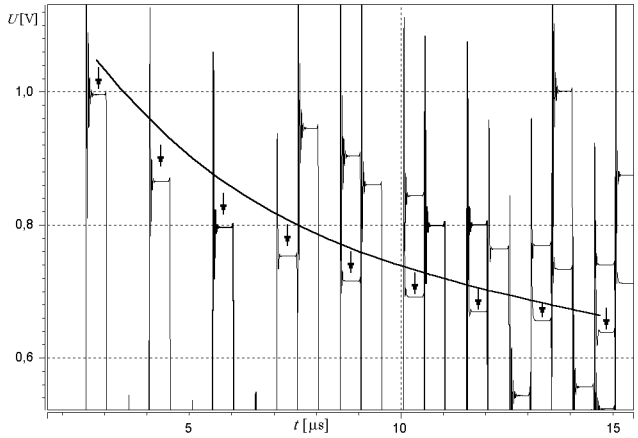


Figure 4.22: Signal along the delay line in the case of improper shapes of clock impulses

Table 4.3: Parameters of different clock systems

Parameter	Even-odd structure $R = 1$	Gillingham structure
Number of D flip-flops	6	1
Number of gates (with output buffers)	56	8
dimensions and the chip area	760x420 μm 0.31 mm^2	350x100 μm 0.035 mm^2

structure, cannot be used, as the signals can be delayed between the phases. Moreover, not all sums of clock signals can be obtained by OR gates. A sum of adjoining phases produced by an OR gate has an unacceptable shape (a transition curve when the counter passes from one stage to another). This is the reason why four phase clock generator (Figure 4.19) consists of six D flip-flops.

The electrical diagram of the clock system is presented in Figure 4.19 for the even-odd delay line structure ($R = 1$). This system fulfills appropriate (mentioned above) time conditions of clock signals. The layout of the clock system for the even-odd delay line structure is presented in Figure 4.23.

In the case of the clock generator for the system with Gillingham delay elements only two phases (complementary signals) are needed. These signals can be obtained by simple "by two divider" connected with gates to separate units and get desirable delays and shapes. Corresponding layout is shown in Figure 4.24 together with layout of the commutation unit (on the right hand side of the Figure). Outputs are connected to this commutation unit, which is a mid-stage between the internal clock generator and the filter structure.

Because of high sensitivity of SC FIR structures to clock signals, pulse shapes and time correlations, transistor dimensions, as well as the right circuit structures, all these parameters were selected and designed very carefully. Each transistor delays the signal, so ways of clock signals should be identical or bring the same delay to avoid clock signal shifts in time.

In Table 4.3 the main parameters of the clock systems for the realized SC FIR filters are shown. Each D flip-flop consists of 26 transistors, a gate with 2 inputs contains 4 transistors, a gate with 3 inputs contains 6 transistors, an inverter consists of 2, and a buffer of 4 transistors [13, 15, 63]. For example, the system shown in Figure 4.19 is composed of 180 transistors (plus additional 100 transistors contained in inverters and buffers at the clock generator outputs).

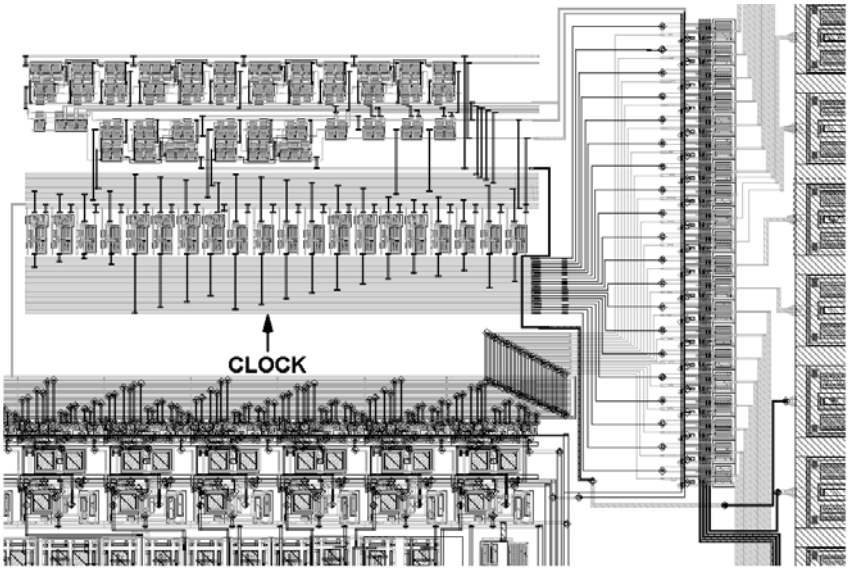


Figure 4.23: Clock signals generator and clock paths for the even-odd delay line structure

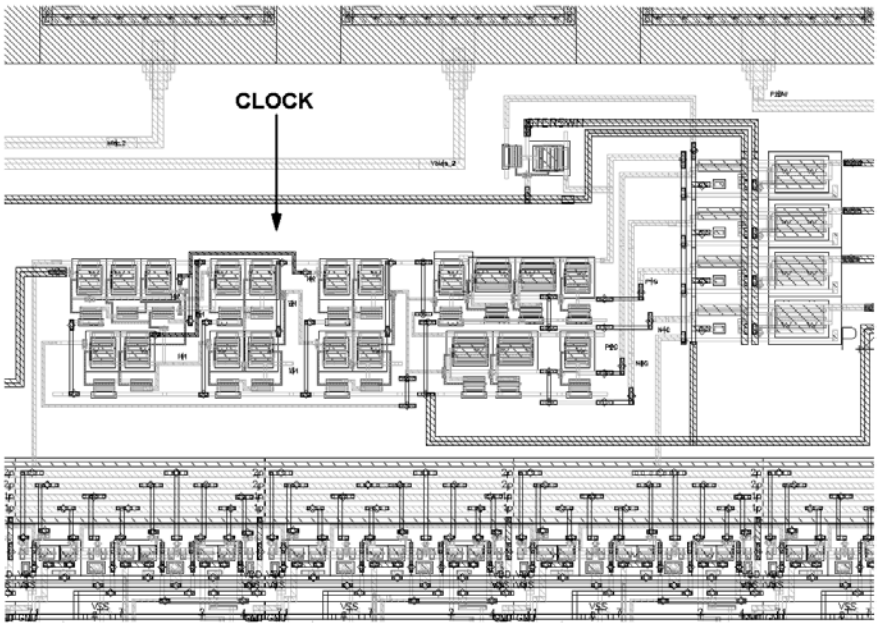


Figure 4.24: Clock signals generator for the Gillingham delay line structure

4.3.2 External clock systems

The first designed and realized filter was an experimental SC FIR filter with Gillingham delay elements [42]. It was driven with an external clock generator only. A simple clock structure such as the one shown in Figure 4.19 (e.g., a structure with D flip-flop 74HC74) is not suitable in this case because no control of shapes, delays, etc. of the pulses would be possible.

A microcontroller AVR AT90S1200 was used instead. It is based on a RISC (reduced instruction set computer) core and most instructions are performed in a single clock cycle [57]. High speed of operation of this microcontroller is realized through the pipelining function. The processor is driven with the 12 MHz clock system (but it works properly also at the frequency of 15 MHz). The minimal time of one instruction is equal to 66.6 ns (under an assumption that the clock frequency is equal to 15 MHz).

Filters with Gillingham delay elements require a two phase clock only, i.e., four physical signals. All these signals are obtainable directly at the microcontroller port. Chosen signals are shown in Figures 4.25 and 4.26. Note that they cross near in the middle of V_{DD} and V_{SS} as required. The falling time is shorter than the rising time but the tested filter is not sensitive to that. Oscillations due to inductances of external connections are also visible. All these problems can be reduced with an internal clock generator.

It is worth stressing that the microcontroller clock is flexible, good for testing and for research purposes but simultaneously too expensive for the final product. Furthermore, in the case of the even-odd delay line structures, rotator structures, and multi-C structures external clock needs a great number of pins. This is another disadvantage of the external clock approach.

To realize the external (microcontroller based) clock generator for the even-odd delay line structure shown in Figure 2.7, an external 20-bit buffer is required (AT90S1200 is 8-bit only). It could be solved by using a DSP or 3 microcontrollelers, but the complexity of such a clock system would be very high.

Reprogrammability of the microcontroller [56] enabled testing of the filter with inserted death-times between clock phases (see Figure 4.27). In order to study the role of death-times an example of the output signal of the second section of the filter is presented in Figure 4.28. The filter in this Figure is driven with the clock with death-times (c.f., Figure 4.27). Next the death-times were reduced to minimum. The corresponding clock diagram is presented in Figure 4.25. The filter output signal obtained in this case is show in Figure 4.29. In comparison to the case with death-times no positive change can be seen, just in the opposite. Thus death-times are in our application (high frequency range) not only unnecessary but even harmful. In the show experiments supply voltage was equal to +/–1.5 V. The current consumed by the structure (I_{DD}=7.05 mA) remains unchanged independently of the existence of death-times. However, in the case without death-times the output voltage can reach higher amplitudes +1.25 V/–1.3 V compared to +1.1 V/–1.25V in the case with death-times. The achievable attenuation also increases without death-times (e.g., for f=300 kHz by 0.6 dB). Thus, the clock

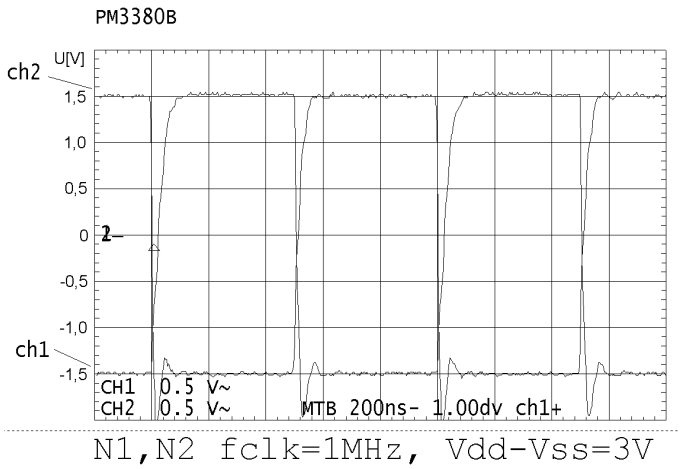


Figure 4.25: Phases N1 and N2 of clock signals for the Gillingham delay line structure generated by an external generator

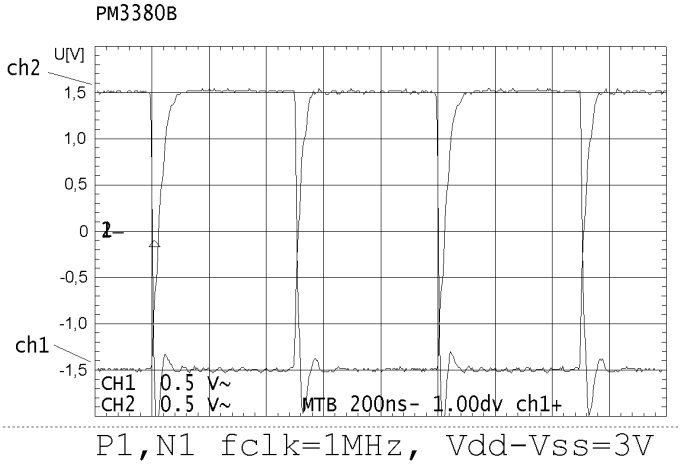


Figure 4.26: Phase 1 of the clock for steering N-type and P-type transistors

system without death-times was chosen. As an example Figure 4.30 illustrates the clock signal, which drives PMOS transistors in the switches.

The described diagrams show that crossing of the clock signal occurs nearly the middle between the maximum and the minimum value. This eliminates situations, in which all switches (driven by different clock phases) are open simultaneously. Clock signals presented in Figure 4.25 minimize also times, in which OA's work with open loops. This minimizes the effect of saturation near to values V_{SS} and V_{DD}.

Measurements presented henceforth were realized with the use of clock signals presented in Figures 4.25 and 4.30.

The clock signals must change in the range of V_{SS} to V_{DD} to make the proper work of the structure possible. The microcontroller drives the structure directly, without other

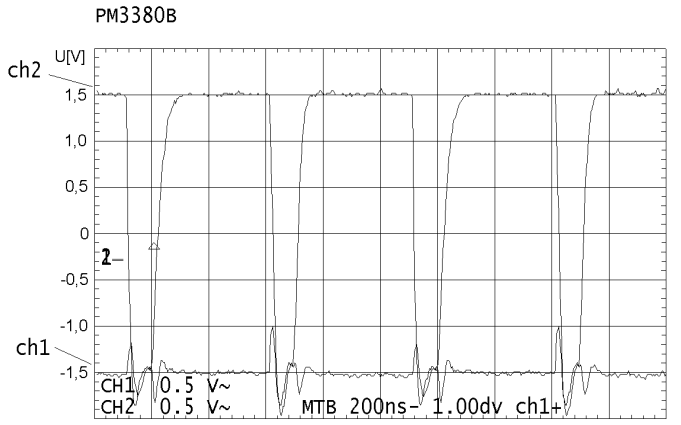


Figure 4.27: Phases N1 and N2 of clock signals with additional death-times for the Gillingham delay line structure

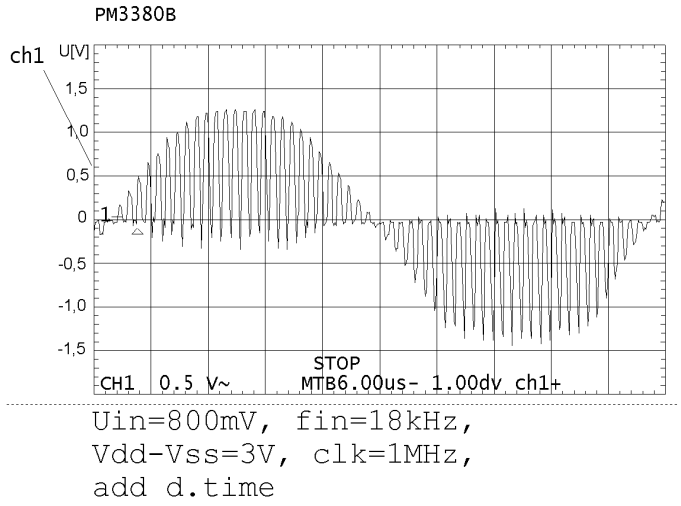


Figure 4.28: The second section output signal (clock signal like in Figure 4.27)

interface elements. Outputs of the chosen microcontroller have sufficient current to drive the switches in the filter. In the above diagrams the amplitude of the clock signals equals to 1.5 V. In general, the clock signals should be not higher than the voltage supply of the filter. That is why in the testing board (c.f., Figure 4.89) additional control of the voltage supply of the microcontroller was implemented. To minimize the signal feedthrough, microcontroller's voltage supply is separated from the voltage supply of the filter structure. The microcontroller works properly with supply voltage at least +/–1.15 V for frequency 12 MHz and with supply voltage +/–1.3 V for frequency 15 MHz. These values contain appropriate margins.

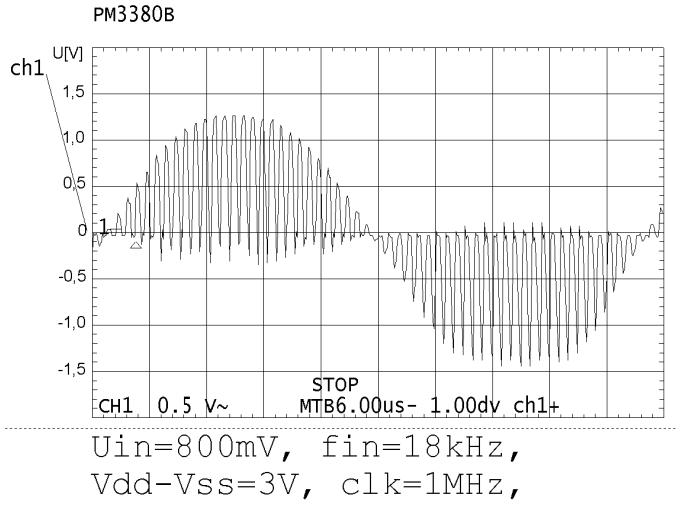


Figure 4.29: The second section output signal (clock signal like in Figure 4.25)

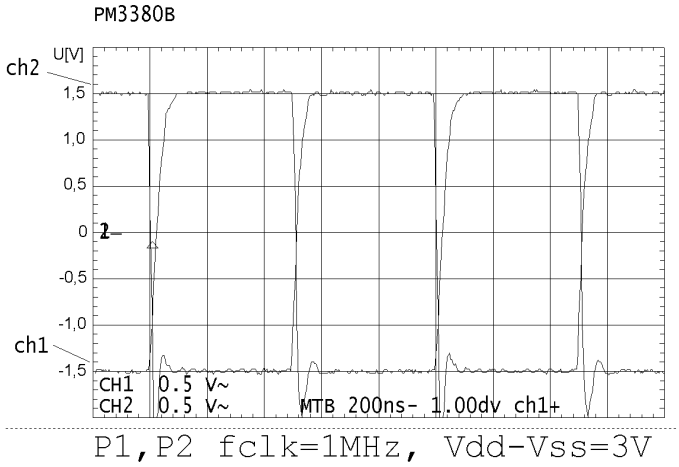


Figure 4.30: Clock signal for PMOS transistors

Summarizing, it can be mentioned that the designer deciding for an internal or for an external clock generator for a given SC FIR filter must consider various conditions:

- how many clock signals are needed,
- how many free pins can be allocated to the clock,
- how many free chip area can be assigned to the clock generator,
- how fast should the system be (external connections bring additional capacitance),
- how large area can the final product occupy (together with external components),

- how much time does the designer have for the project,
- what is the required flexibility of the system,
- what costs are acceptable.

It should also be mentioned that mixed clock systems are also possible. Some parts of the clock generator can be placed in the chip (e.g., OR gates) while some other parts can be connected externally.

An important feature of the designed chips is a possibility of connecting internal clock system signals to the chip output pins in order to test them and measure. These pins can also be used as a clock generator for other purposes.

4.4 First prototype of the GSM channel filter

4.4.1 Design of filter layout

Optimization of the filter coefficients, preliminary PSPICE and HSPICE Simulations, and other supplementary calculations gave us enough information about the appropriate circuit parameters and allowed us to design the layout. The most important problem was the proper choice of the transistor dimensions and of the capacitor values. The project was realized in the CMOS 0.8 μm technology using the CADENCE software environment [55, 64]. The area of the entire circuit is equal to about 2.3 mm^2 and exactly agrees with the theory [34].

The placement of particular building elements (described in Section 4.2) is the result of the multi-criteria optimization.

SC FIR filters are mixed integrated circuits, with digital and analog parts. Such a combination may cause the signals from a digital part (in our case the clock signals) to influence the effective signal in the analog part. Because of this, the most sensitive analog elements have to be placed at the longest possible distance from the clock paths. Such a strategy allows us to separate analog and digital elements. Since the switches are driven directly by the clock pulses, they must be placed near to the clock paths, but the capacitors and OA's are placed far from the clock paths. To avoid clock feedthrough into the analog part, an additional protection is used by the placement of sensitive elements in special areas separated from the other parts of the circuit by a voltage barrier. Due to this protection we can eliminate or at least minimize parasitic charge flows, which can induce errors by introducing additional parasitic charges to capacitors. Because of that, CC's and clock paths are placed on different n-wells, connected to the V_{DD} voltage. The filter layout is shown in Figure 4.31. Elements are placed in the structure in a specific schema, which is presented in Figure 3.31.

In Figure 4.32 a part of the delay line with Gillingham delay elements is shown. Note that operational amplifiers are placed at the top of the layout in Figure 4.32. In Figure 4.33 the layout of coefficient capacitors is shown. In Figure 4.34 we see a part of the

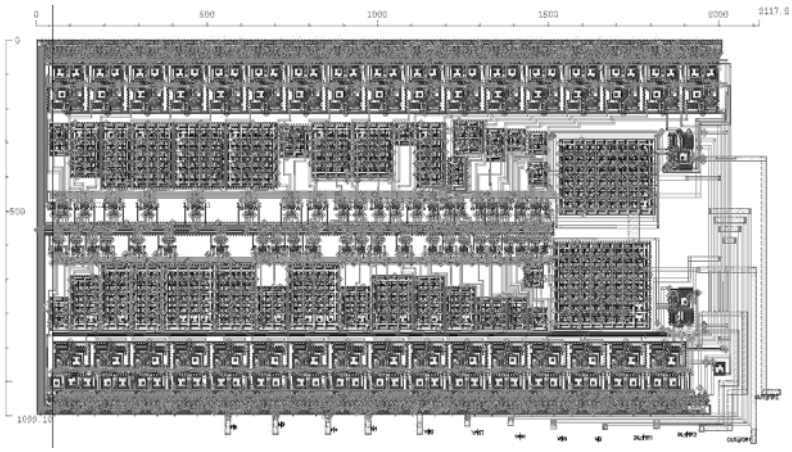


Figure 4.31: Layout of the GSM channel FIR filter of order $N = 31$

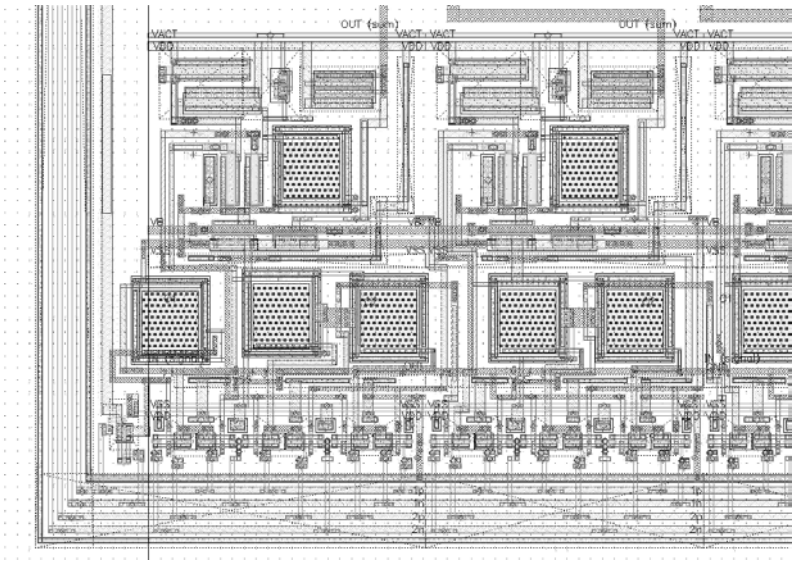


Figure 4.32: A part of the delay line layout

line with the switches in the summer circuit and in Figure 4.35 the OA at the output of the filter is shown.

The next important step was verification of the designed circuit. We have to check correctness of the layout as well as functionality of the circuit. This was made in the HSPICE environment using the extraction facility for circuit parameters. Especially important is the verification of the circuit attenuation in the stopband, as the passband attenuation is usually less sensitive to different imperfections of the circuit elements and parasitic capacities.

Illustrative waveforms of the effective (output) signals are shown in Figure 4.36a in the passband and in Figure 4.36b in the stopband. In Figure 4.36a two different output signals are plotted: the output signal of the first section and the output signal of the

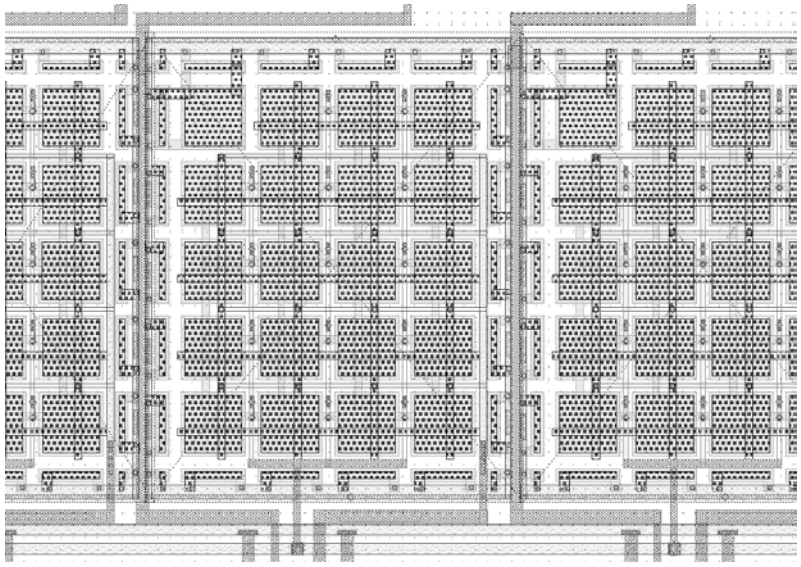


Figure 4.33: A part of the layout of coefficient capacitors

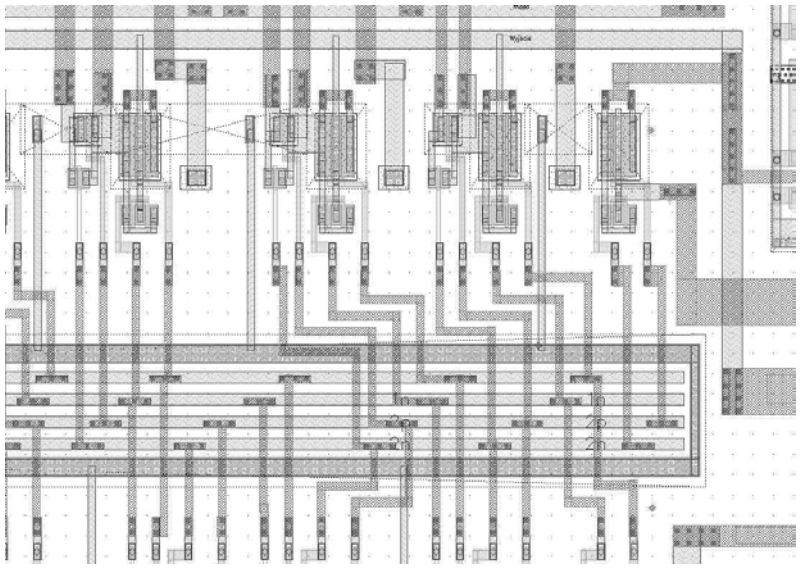


Figure 4.34: Switches in the summer circuit

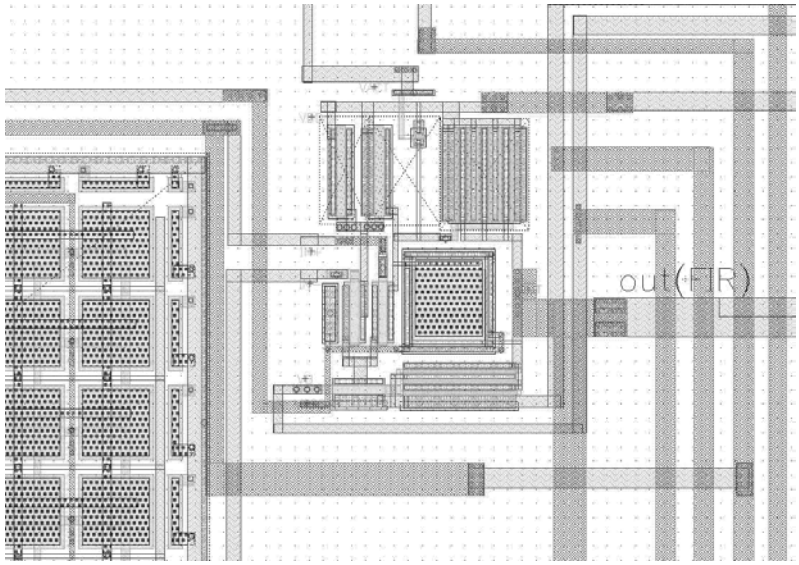


Figure 4.35: Operational amplifier at the output of the filter

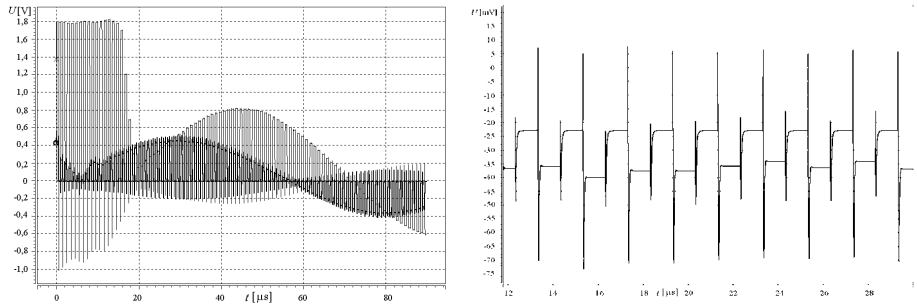


Figure 4.36: Effective (output) signals in: (a) passband (b) stopband

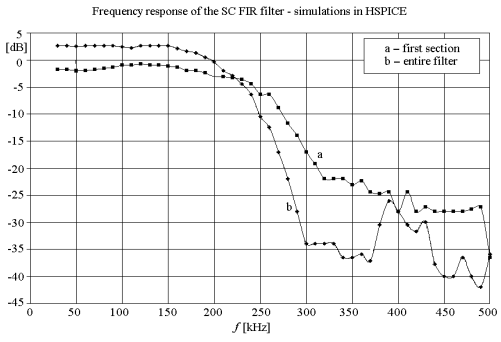


Figure 4.37: Frequency response of the first section and of the entire filter

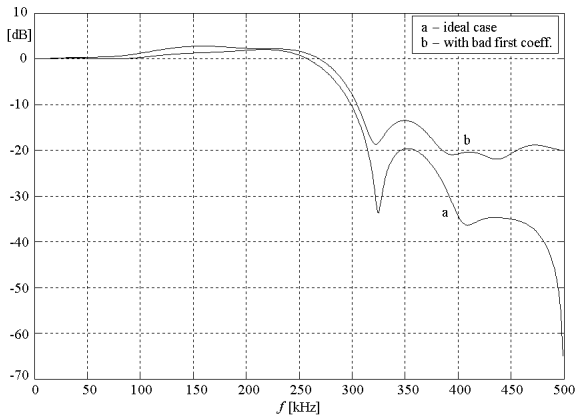


Figure 4.38: Influence of the changed sign of the first coefficient on the frequency response of the filter: (a) correct case, (b) incorrect case

entire filter, i.e., the signal at output of the second section. The input signal was a sinusoidal voltage with the amplitude of 0.5 V and the frequency of 10 kHz (passband). The frequency response of the first section as well as of the entire filter is shown in Figure 4.37.

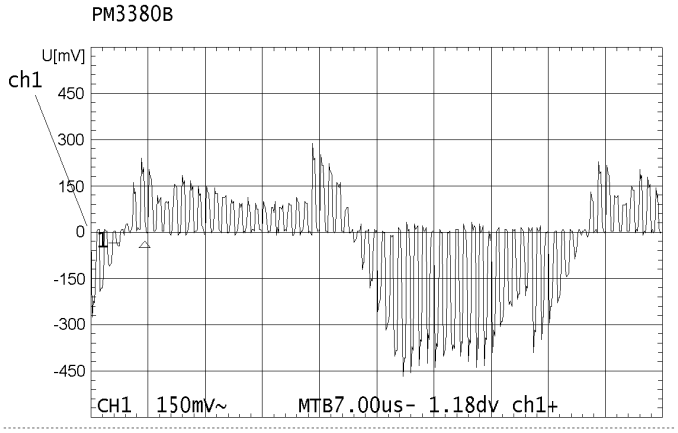
The layouts presented in Figures 4.31–4.35 are those of the first prototype of the GSM channel filter. In this project there appeared two errors, both in the first section of the filter. One of them consisted in the change of the sign of one of the coefficients, which influences the frequency response (c.f., Figure 4.38). However, this error is not critical. Far more serious is the second error. One of switches in the delay line was connected to the clock path in a wrong way so that the first section does not work properly. These errors were removed in the second prototype (see Subsection 4.5).

4.4.2 Chip measurements

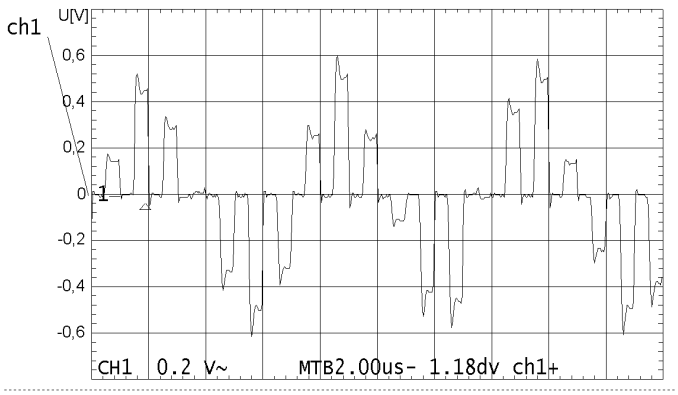
Measurements of the frequency response of the channel filter

The investigated filter is the low-pass filter. It is driven by the 1 MHz clock system. The upper signal frequency is equal to 500 kHz. The measurements were realized in the optimal conditions, i.e., optimal bias voltage and with the optimal clock signals (see Section 4.3). The first section does not work properly. The output signals with frequencies below 100 kHz are heavily distorted and this section is not satisfactorily selective in these frequencies (c.f., Figure 4.39a). In the upper frequencies the situation is slightly better (c.f., Figure 4.39b, c), but the frequency response is far from the theoretical curve (c.f., Figure 4.40).

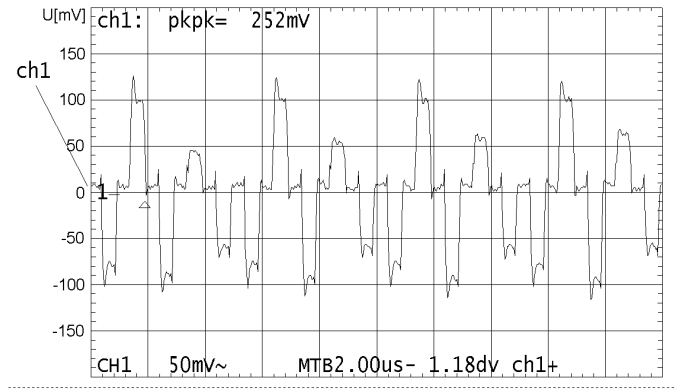
On the contrary, the second filter section works perfectly. Illustrative time diagrams for the supply voltage equal to 3 V are shown in Figures 4.41 and 4.42. There is no visible distortion of the harmonic output signal in the whole frequency range, i.e., for frequencies up to 500 MHz. Illustrative output signals for different input signal



I, Uin=700mV, fin=18kHz, Vdd-Vss=5V, clk=1MHz



I, Uin=700mV, fin=150kHz, Vdd-Vss=5V, clk=1MHz



I, Uin=700mV, fin=400kHz, Vdd-Vss=5V, clk=1MHz

Figure 4.39: Output signal after the first section for the input signal of frequency: (a) 18 kHz, (b) 150 kHz , (c) 400 kHz

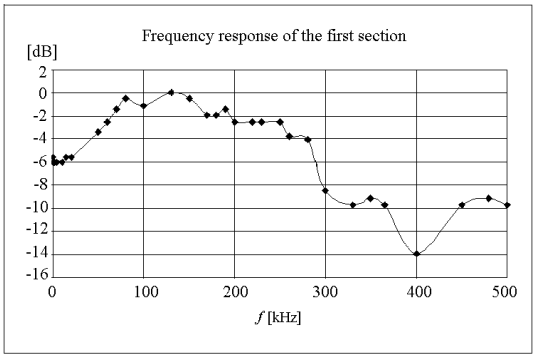


Figure 4.40: Frequency response of the first section with parameters: U_{in} = 2 Vpp, f_{clk} = 1 MHz, V_{DD} = 2.5 V, V_{B} = −1.0 V

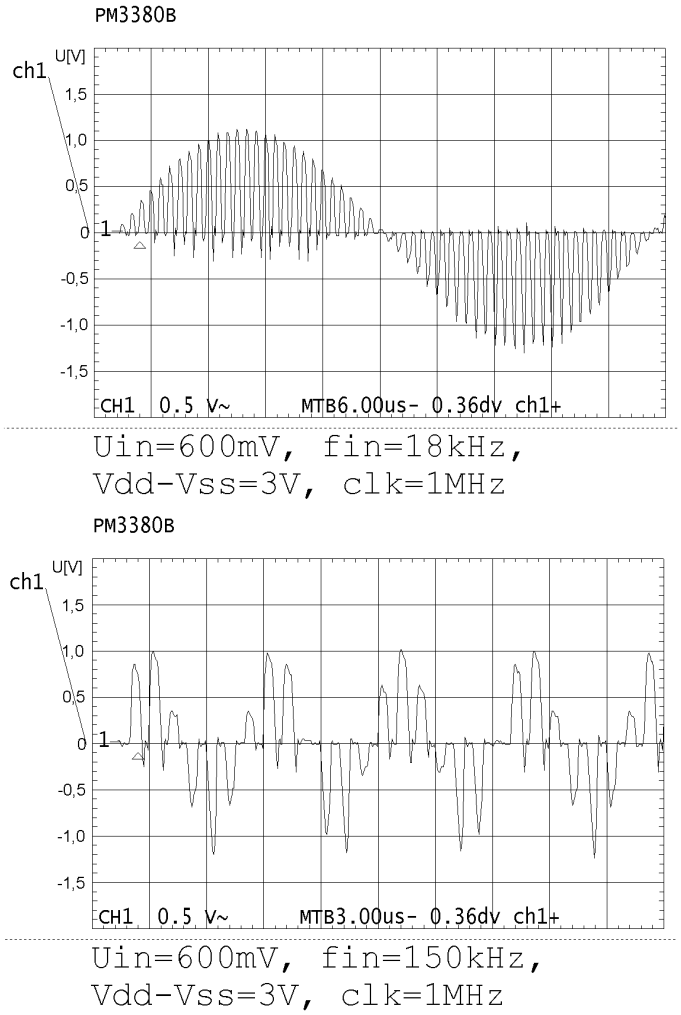


Figure 4.41: Output signal after the second section for the input signal of frequency: (a) 18 kHz, (b) 150 kHz

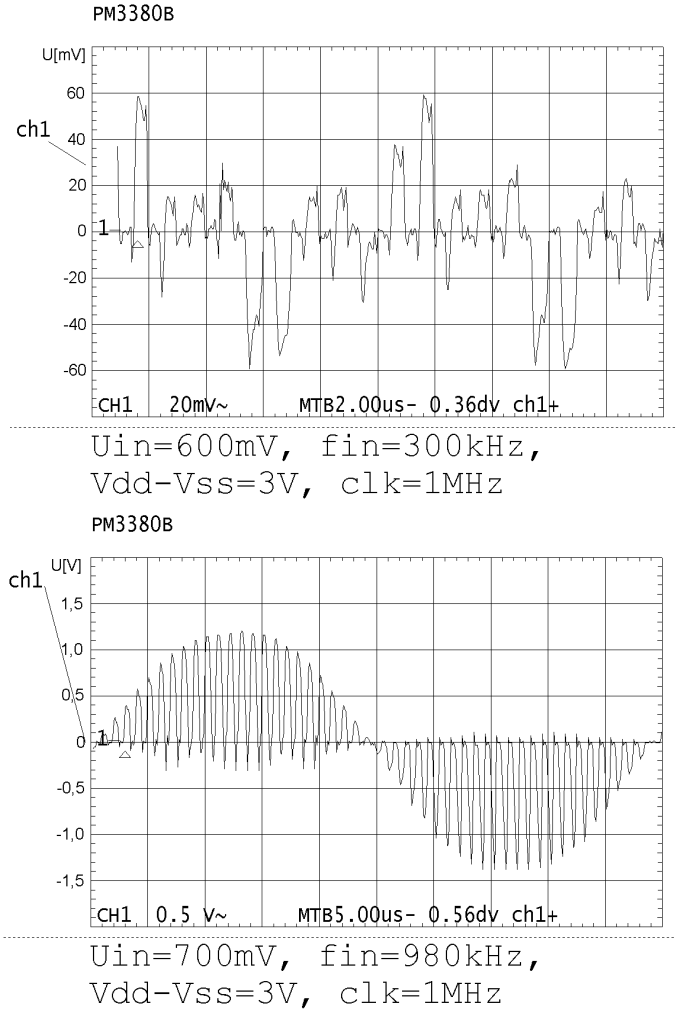


Figure 4.42: Output signal after the second section for the input signal of frequency: (a) 300 kHz, (b) 980 kHz

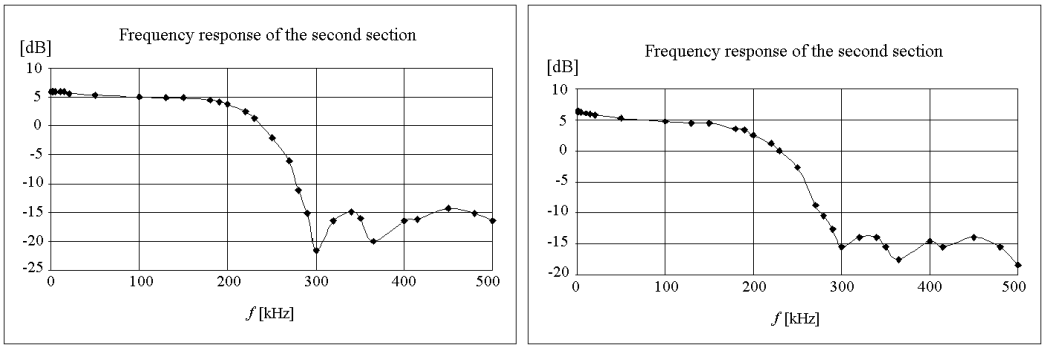


Figure 4.43: Frequency response of the second section for $f_{\mathrm{clk}} = 1$ MHz, $V_{\mathrm{DD}} = 2.5$ V, $V_{\mathrm{B}} = -1.0$ V: (a) $U_{\mathrm{in}} = 2$ Vpp, (b) $U_{\mathrm{in}} = 150$ mVpp

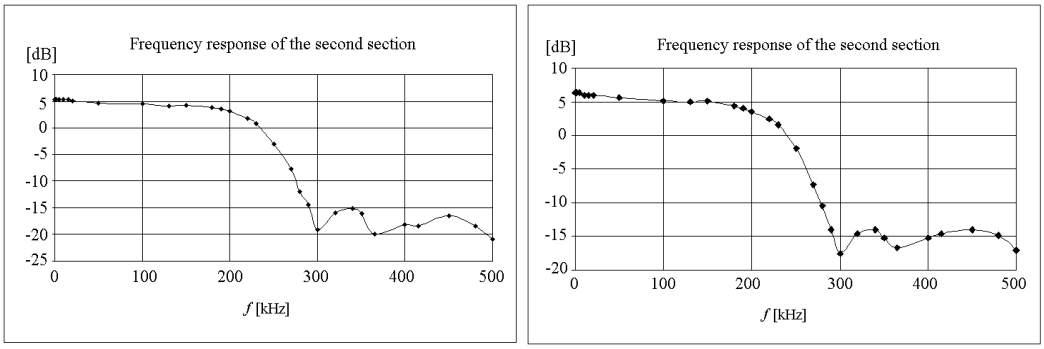


Figure 4.44: Frequency response of the second section for: $f_{\mathrm{clk}} = 1$ MHz, $V_{\mathrm{DD}} = 1.5$ V, $V_{\mathrm{B}} = -0.39$ V: (a) $U_{\mathrm{in}} = 1.2$ Vpp, (b) $U_{\mathrm{in}} = 150$ mVpp

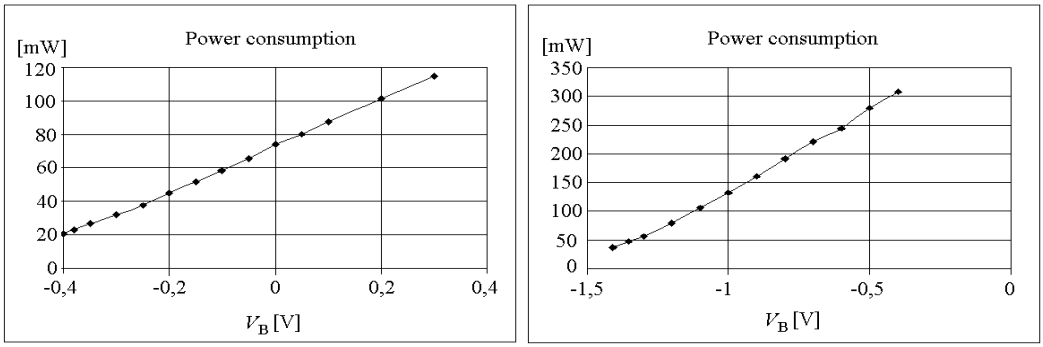


Figure 4.45: Power consumption as a function of the bias voltage V_{B} for: (a) supply voltage V_{DD}=1.5 V, (b) supply voltage V_{DD}=2.5 V

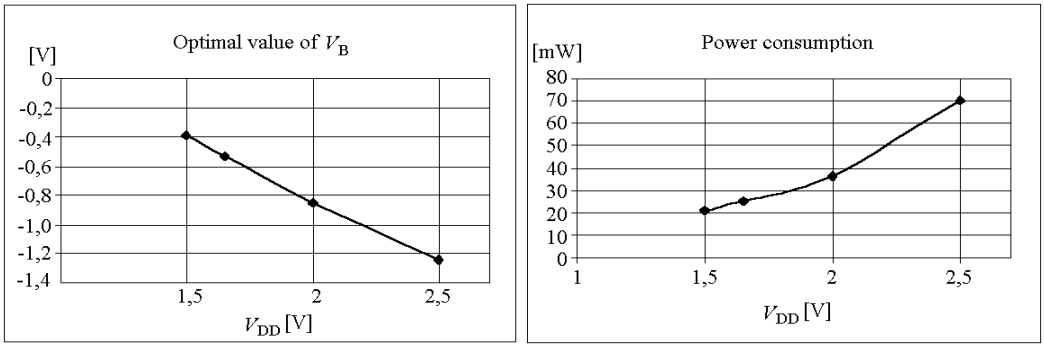


Figure 4.46: Additional parameters: (a) optimal value of the bias voltage V_{B} and (b) power consumption for the optimal value of V_{B} as functions of the supply voltage V_{DD}

frequencies are presented in Figures 4.41 and 4.42. In the passband the amplitude of the output signal is the same as the amplitude of the input signal. Figure 4.42 shows, that for the frequency of 980 kHz the signal is identical to that of 20 kHz (1 MHz–980 kHz) as it results from the theory.

In Figures 4.43 and 4.44 we present measured frequency responses of the second filter section. Measurements were made with various supply voltages. Results for the supply voltage of 5 V are shown in Figure 4.43 while those for 3 V — in Figure 4.44. Figures labeled with (a) show frequency responses for large input signals, i.e.: 2 Vpp for V_{DD}=2.5 V and 1.2 Vpp for V_{DD}=1.5 V, respectively. On the contrary, for comparison, Figures labeled with (b) are added. They correspond to a small input signal of 150 mVpp. In all cases the measured responses perfect.

Comparison of various frequency responses for the second filter section is important, because it has to operate with much greater dynamic range than the first section. For example, input signal of 0.15 Vpp simulates, for the supply voltage equal to 5 V, attenuation of the first section of about 30 dB (for the frequency 500 kHz this attenuation should be equal to ca. 25 dB). It should be stressed that the second section is much more important for the overall filter performance than the first section. That is why the whole filter operates satisfactorily well although the first section alone does not.

Measurements of the power consumption

Another important parameter is the power consumption of the entire filter. This value depends, in general, on two parameters: the supply voltage $V_{DD} - V_{SS}$ and the bias voltage V_B of OA's. Both voltages are also responsible for the quality of the output signal. That is why not only the power consumption but also the output signal distortion were measured. The results are presented in Figures 4.45, 4.46 and 4.47. It can be seen that we very fortunately obtain the optimal (symmetric) output signal just for the V_B value, which minimizes the power consumption. Decreasing the supply voltage V_{DD} from 2.5 V to 1.5 V (with optimal parameters) reduces the power consumptions by almost 3.5 times.

Figures 4.48, 4.49 (and 4.50 for V_{DD} = 2.5 V) show that a non-optimal bias voltage V_B reduces the maximum amplitude of the output signal and introduces the non-symmetry to the signal, especially if the amplitude is high (the higher the amplitude the higher is the non-symmetry — see Figure 4.50). Figure 4.49 shows that for low amplitudes the non symmetry is low.

However, the value of the bias voltage V_B, which is optimal for the low power consumption and the signal symmetry, differs from the optimal value of V_B for the output signal slopes. This problem is illustrated in Figure 4.48b and 4.49a.

In practice, the value of V_B that is optimal for the signal symmetry was chosen. With this value the power consumption is minimized, but the output signals slopes are not optimal, they are, however, acceptable.

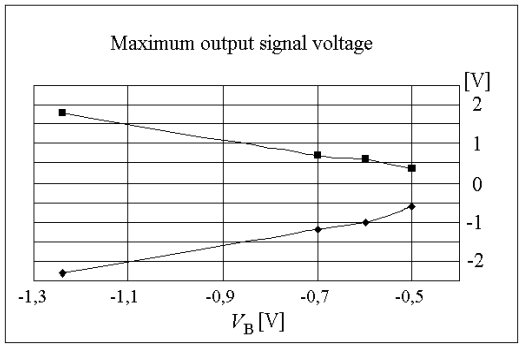


Figure 4.47: Maximum not distorted output signal as a function of the bias voltage V_B for $V_{DD} = 2.5$ V

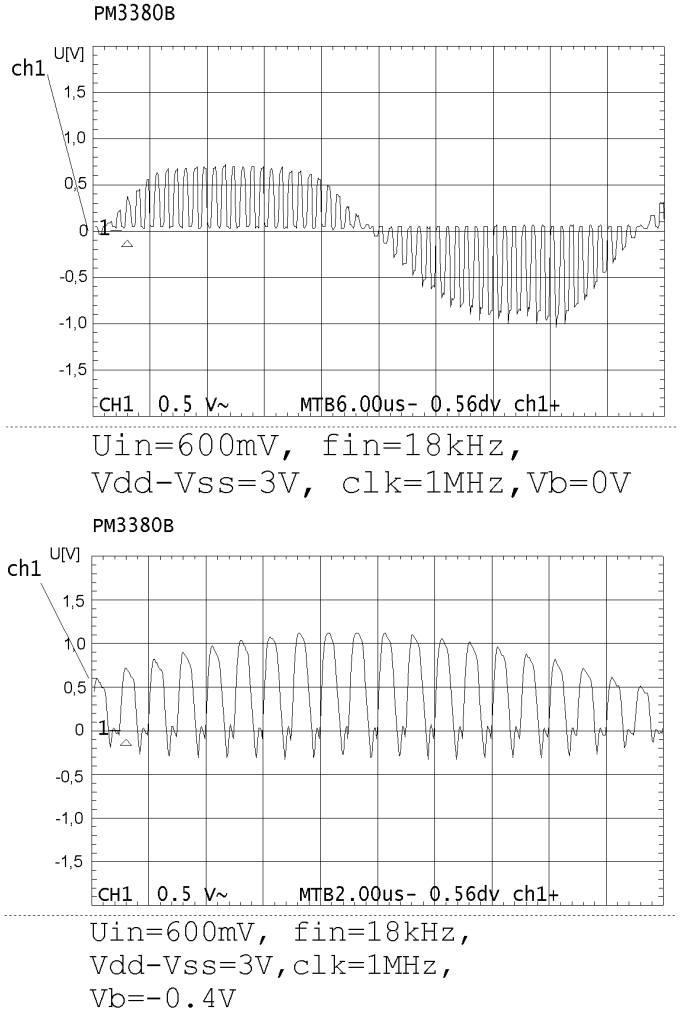
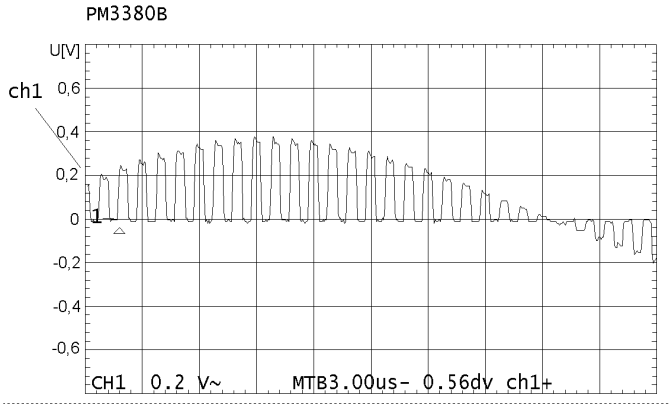
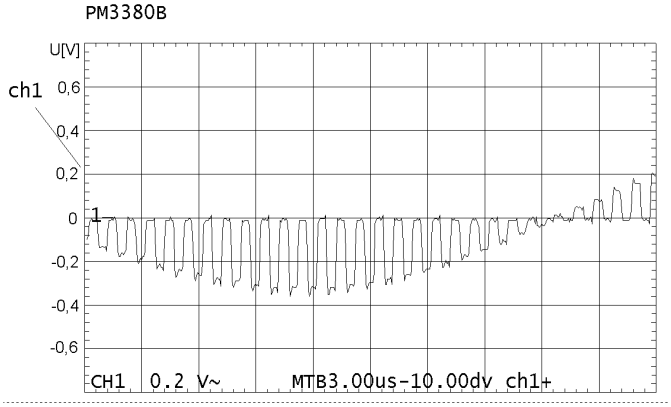


Figure 4.48: Second section output signal by: (a) unoptimal V_B, (b) optimal V_B



Uin=200mV, fin=18kHz,
Vdd-Vss=3V,clk=1MHz,
Vb=0V



Uin=200mV, fin=18kHz,
Vdd-Vss=3V,clk=1MHz,
Vb=0V

Figure 4.49: Output signal of the second section with non optimal V_{B} and: (a) values greater than zero, (b) values less than zero

The measurements show that the increase of the V_B by 0.5 V above the optimal value, increases the maximum attenuation by 1.5 dB. However, increasing V_B by 0.7 V decreases the attenuation by 5.5 dB.

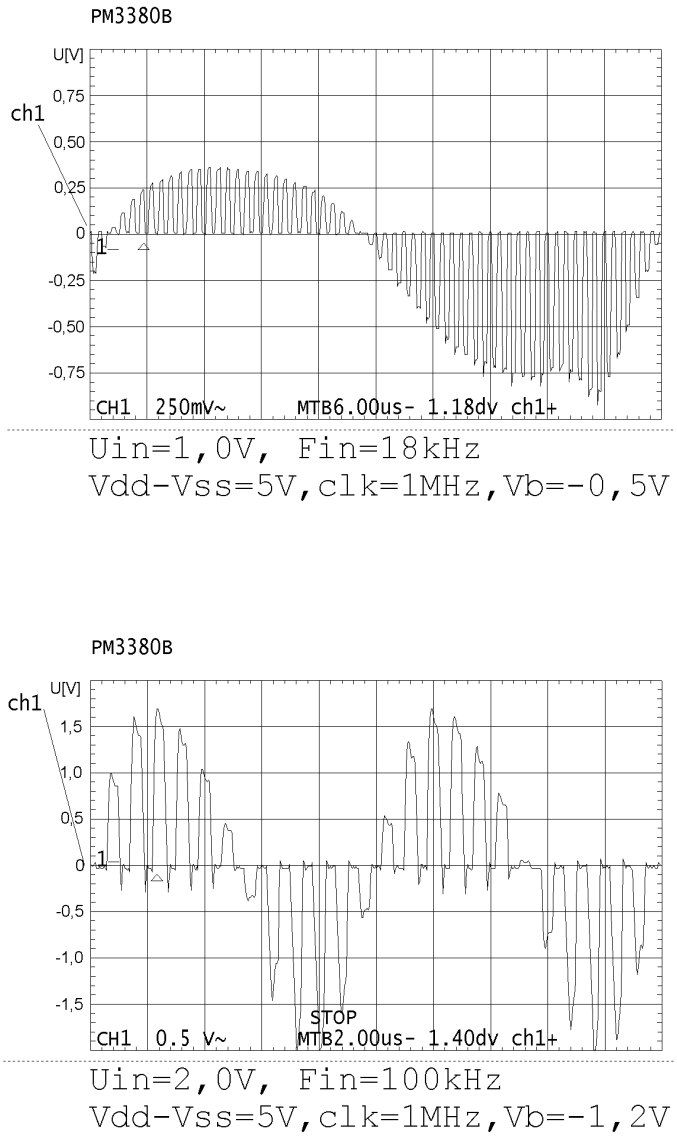


Figure 4.50: Output signal of the second section with: (a) non optimal V_B and frequency of the output signal equal to 18 kHz, (b) near optimal V_B and frequency of the output signal equal to 100 kHz.

The V_{ACT} signal is used to switch on/off of the OA's and in consequence the entire structure. Switching off causes that the power consumption decreases to 18 mW (for $V_{DD} = 2.5$ V) and to 2 mW (for $V_{DD} = 1.5$ V). These values do not depend on other control signals in the structure.

Measurements of the filter with the 2 and 2.5 MHz clock

To check the maximum chip rates, the designed filter was also tested with the clock frequencies 2 MHz and 2.5 MHz. In these cases the frequency responses should be scaled up, but that fact is not of primarily importance for the test. The tests shows that for low signal amplitudes the structure works correctly (c.f., Figure 4.51) even for $f_{\mathrm{clk}} = 2.5$ MHz. The power consumption remains constant in both cases.

Unfortunately, for $V_{\mathrm{DD}} = 1.5$ V the structure is already too slow. In Figure 4.52 it can be seen that the time, in which the output signal reaches zero is absent (compare with Figure 4.51). Increasing the clock frequency radically decreases the dynamic range of the structure, i.e., the maximum amplitude of the signal, whose values lower than zero are not distorted. This is illustrated in Figure 4.53. These effects result from insufficiently steep slopes of the output voltage.

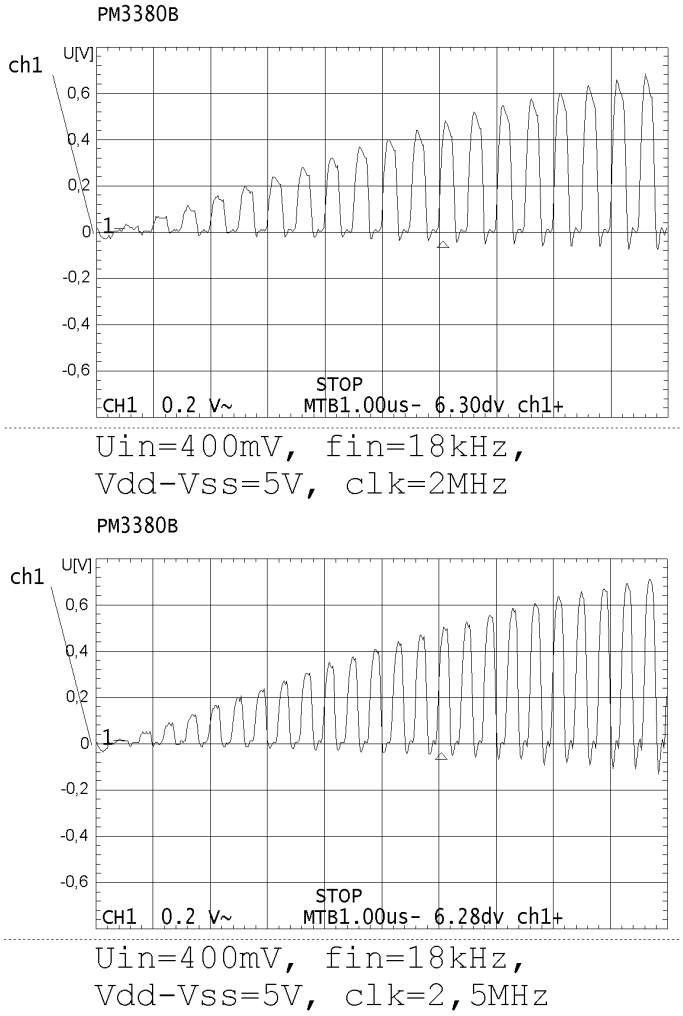
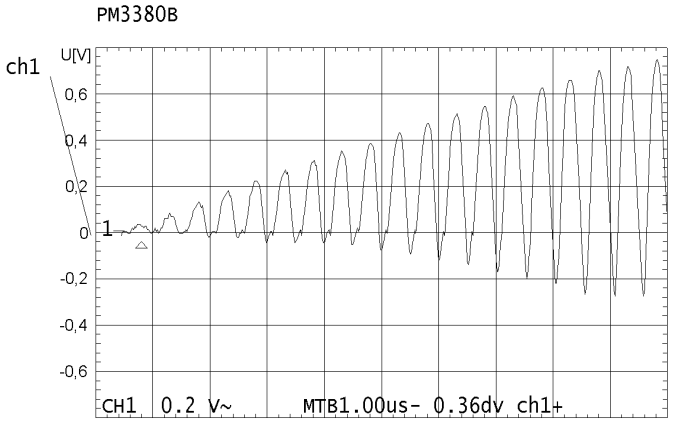
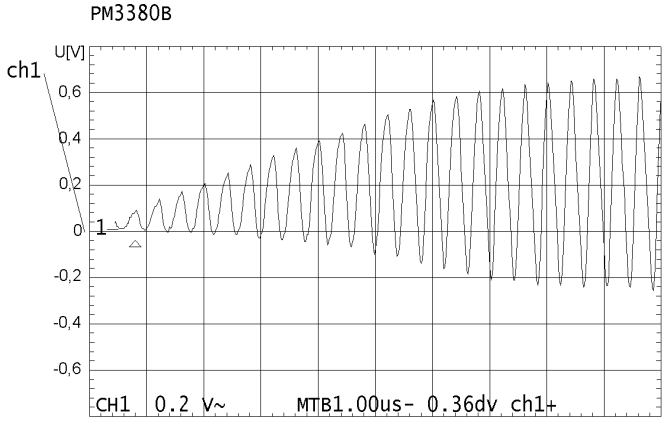


Figure 4.51: Output signal of the second section for parameters: amplitude of the output signal 400 mV, $V_{\mathrm{DD}} = 2.5$ V and: (a) $f_{\mathrm{clk}} = 2$ MHz, (b) $f_{\mathrm{clk}} = 2.5$ MHz

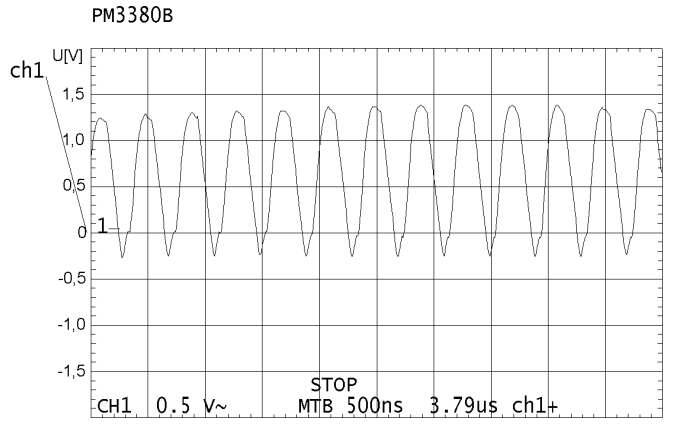


Uin=400mV, fin=18kHz,
Vdd-Vss=3V, clk=2MHz

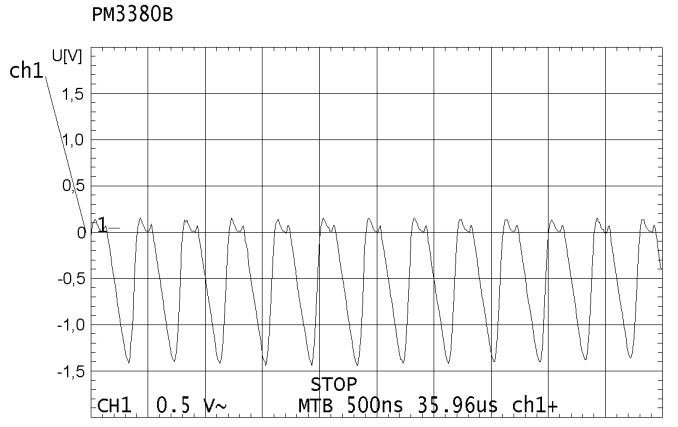


Uin=400mV, fin=18kHz,
Vdd-Vss=3V, clk=2.5MHz

Figure 4.52: Output signal of the second section for parameters: amplitude of the output signal 400 mV, $V_{\mathrm{DD}} = 1.5$ V and: (a) $f_{\mathrm{clk}} = 2$ MHz, (b) $f_{\mathrm{clk}} = 2.5$ MHz



Uin=700mV, fin=18kHz,
Vdd-Vss=5V, clk=2,5MHz



Uin=700mV, fin=18kHz,
Vdd-Vss=5V, clk=2,5MHz

Figure 4.53: Output signal of the second section for parameters: amplitude of the output signal 700 mV, V_{DD} = 2.5 V: (a) negative signal values, (b) positive signal values

4.5 Second prototype of the GSM channel filter

In this Section we present a project of an integrated circuit with two SC FIR filters, namely:

- the optimized version of the filter realized previously and just described (based on the Gillingham delay elements) and
- the filter based on the even-odd delay line structure of order $R = 1$.

Additionally, switching circuits are realized, which make it possible to drive the filters with an external or an internal clock (see Section 4.3).

4.5.1 Design of the layout

Chip presented in this Section, similarly to the first SC FIR filter prototype was designed and fabricated in the CMOS CYE 0.8 μm technology [47] in cooperation with the EUROPRACTICE organization.

Layout of the entire chip is shown in Figure 4.54. The chip contains separated blocks designed by two Divisions of two Universities. A part visible on the left hand side is composed of blocks designed in the group of Prof. Ryszard Wojtyna, from the Academy of Technology and Agriculture in Bydgoszcz. A part visible on the right hand side contains blocks designed by author of this dissertation at the Poznan University of Technology.

The upper right block, which is zoomed in Figure 4.55, is an improved version of the filter with the Gillingham delay elements. Placement of the blocks in this structure is almost the same as in the first prototype. The difference, in comparison to the first prototype, presented in Section 4.4, consists in changed dimensions of some transistors, changed placement of some signal paths and correction of errors. These changes are, in practice, invisible in the layout diagrams shown in the publishing scale.

The lower right block in Figure 4.54 is a filter with the "even" and "odd" delay elements (zoomed in Figure 4.56). The linear dimensions of the even-odd delay line filter are equal to 1550x1500 μm. In result the area is nearly to 2.4 mm^2. In Figures 4.57 and 4.58 a part of the delay line with even and odd delay elements and a part of the summer circuit, respectively, are presented.

In the middle of Figure 4.58 clock paths are visible. Over and below of them switches are placed. Their dimensions are bigger than those of the delay line switches. This is because it is necessary to minimize time constants. Charges from the coefficient capacitors are carried (through these switches) into a large output (feedback) capacitor (placed on the right hand side). If time constants are low, then the recharging process is quick and the resulting maximum signal frequency is sufficiently high.

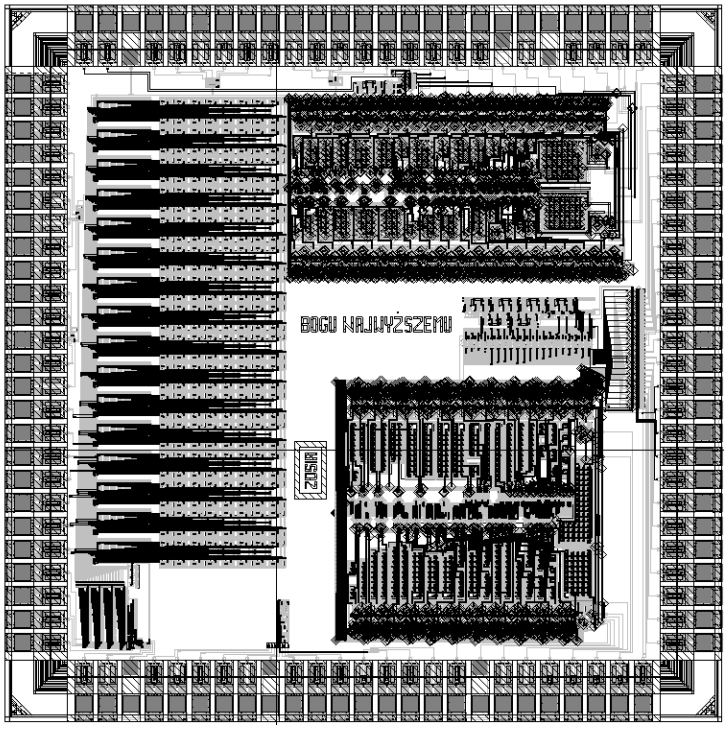


Figure 4.54: Layout of the entire chip

Both filters were designed to work with a completely separated power supply and clock signals. Filters can be driven in two ways: by an internal or by an external clock system (see Section 4.3).

Before starting of the technological process, layouts of the filters were carefully tested and optimized use simulations in the HSPICE environment. It is worth noting that the obtained curves closely agree with the theory. The stopband attenuation of the entire structure is, however, slightly worse than the theoretical value. This is an effect of the structural noise and of other inaccuracies, which degrade the filter frequency response. There are also some other error sources. Among them are: clock jitter and inaccuracies of switches. Other error sources result from the transmission of signal samples along the delay line. Output voltages, which represent the signal samples, decrease after each delay element.

Initial file to perform simulations is he netlist file generated by the CADENCE environment and it consists of all desirable components (e.g., transistors, wires, capacitors) and also parasitic elements (e.g., capacities).

In Figure 4.59 a waveform of the output signal of the even-odd delay line structure is shown. The signal frequency is equal to 240 kHz, which is in the beginning of the transition band, i.e., almost in the midrange the filter frequency response. It is worth noting that this waveform is perfect with a large margin of correct operation toward higher frequencies.

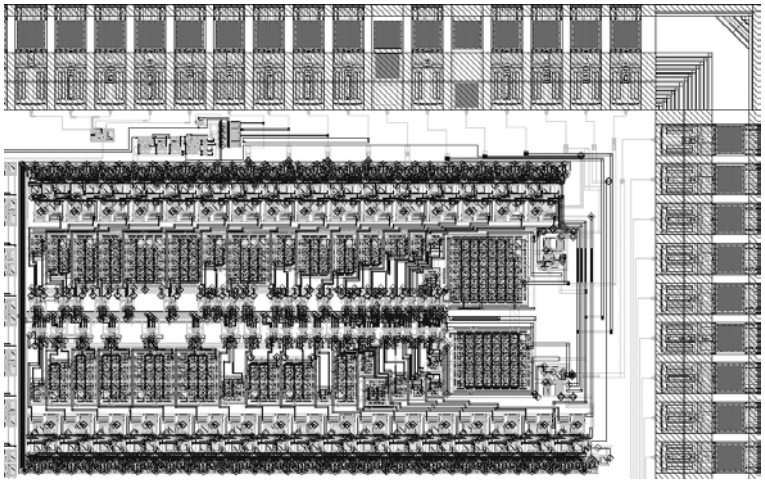


Figure 4.55: Layout of the Gillingham delay line structure

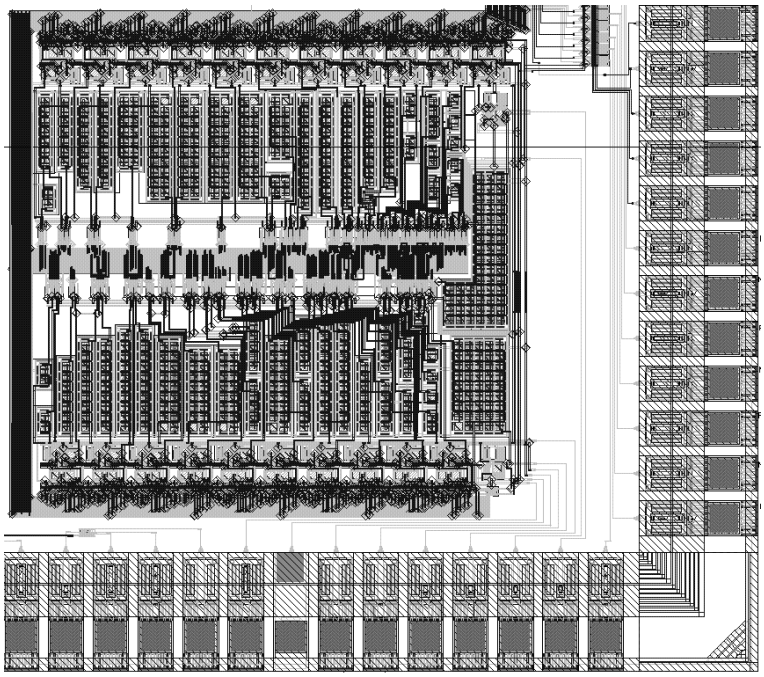


Figure 4.56: Layout of the even-odd delay line structure

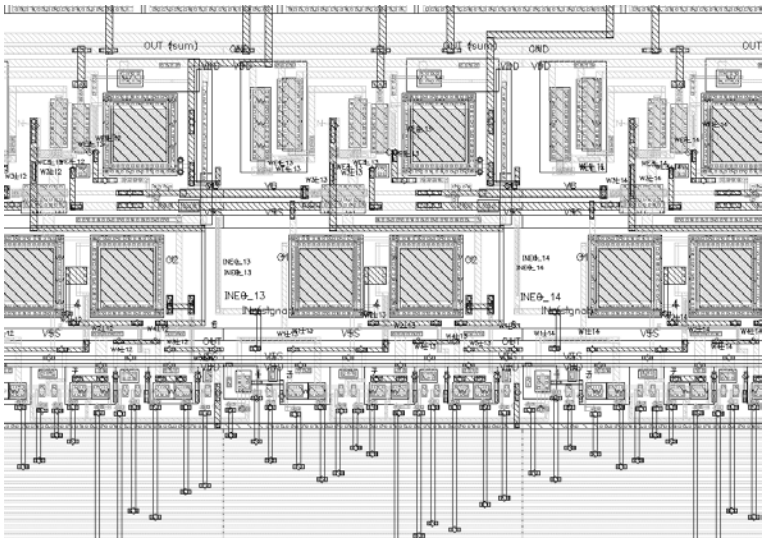


Figure 4.57: Layout of the even and odd delay elements

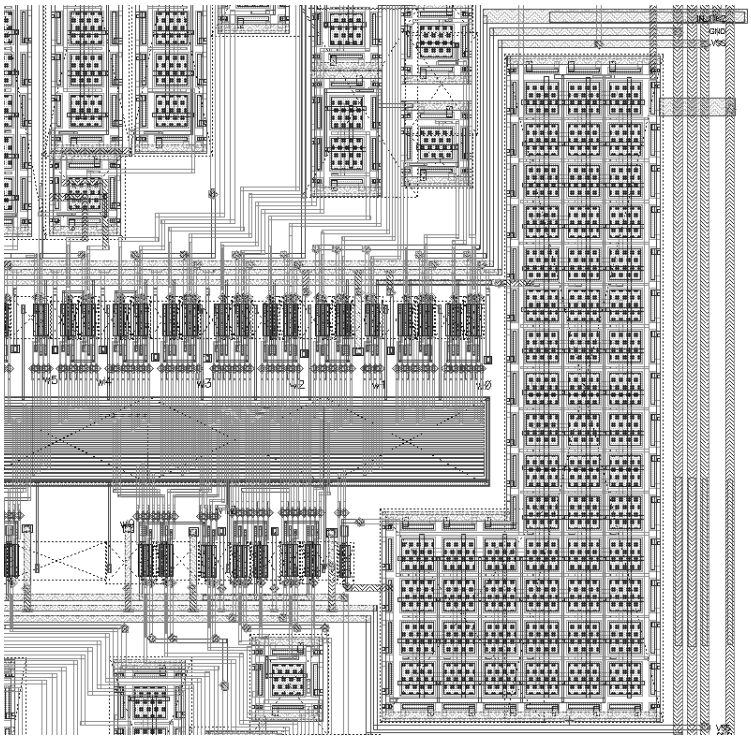


Figure 4.58: Layout of the summer circuit

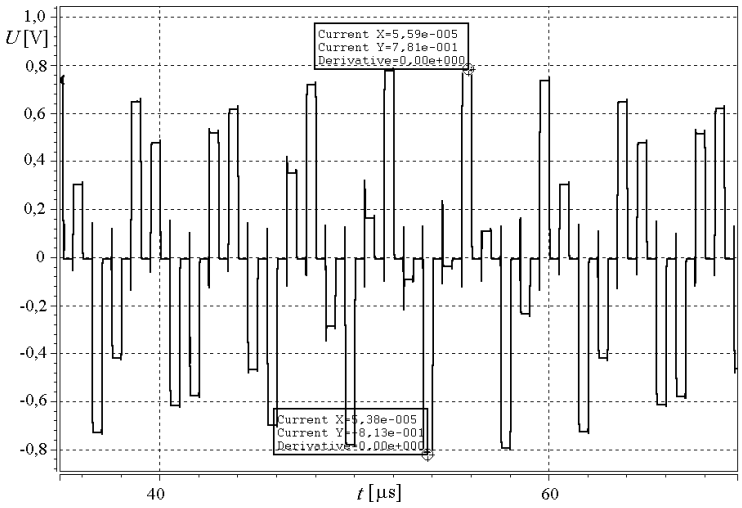


Figure 4.59: Output signal of the even-odd delay line structure for $f = 240$ kHz (midrange)

Simulated frequency responses of particular sections of both filter versions: the filter with Gillingham delay elements and the filter with even-odd delay elements are shown in Figures 4.60 (the first section) and 4.61 (the second section). By analysis and comparison of these curves we conclude that both filter versions almost equally well fulfill the requirements.

An interesting aspect of the whole design process was optimization of the final frequency response by precise control of parasitic effects and by studying their influence on the filtering properties. It can be affirmed that not every parasitic component is equally significant. Some of them can in specific situations be even useful (e.g., capacitances between the power supply lines). The others can be really harmful for the quality of the signal processing.

It turned out that the critical points in our filters are parasitic capacitances between inputs and outputs of delay elements and also between connections inside the delay elements. We observed that these capacitances cause a substantial voltage fall in the samples rewritten along the delay line. This is illustrated in Figure 4.62. The fall at the end of the whole line can be quite large and can drastically change the frequency response of the filter (c.f., Figure 4.63).

It should be seen that the attenuation in the stopband is not simply the sum of attenuations of both sections. It is because in the stopband the structure works with small signals near the noise floor and even little errors in signal processing are visible at the output.

A problem is also the required smoothness of the passband. A solution of this problem was replacement of significant components and move of connections between them but also elimination of critical crosses of wires. After several loops of optimizations and

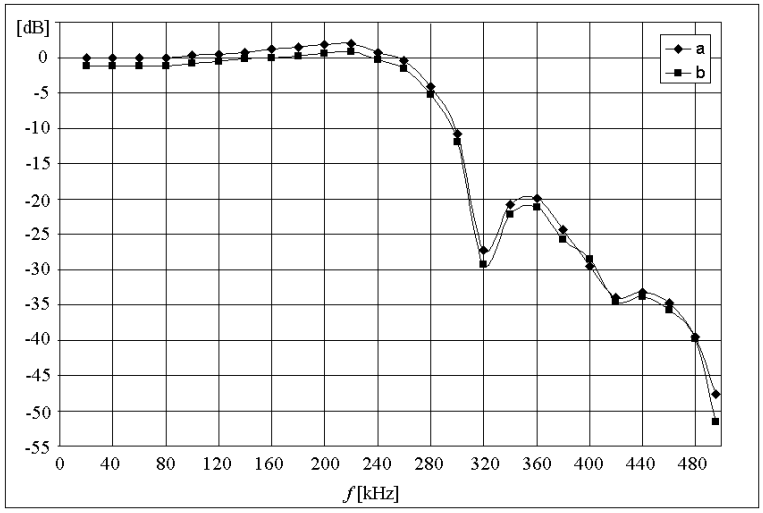


Figure 4.60: Frequency response of the first section: (a) of the structure with even-odd delay elements, (b) of the structure with Gillingham delay elements

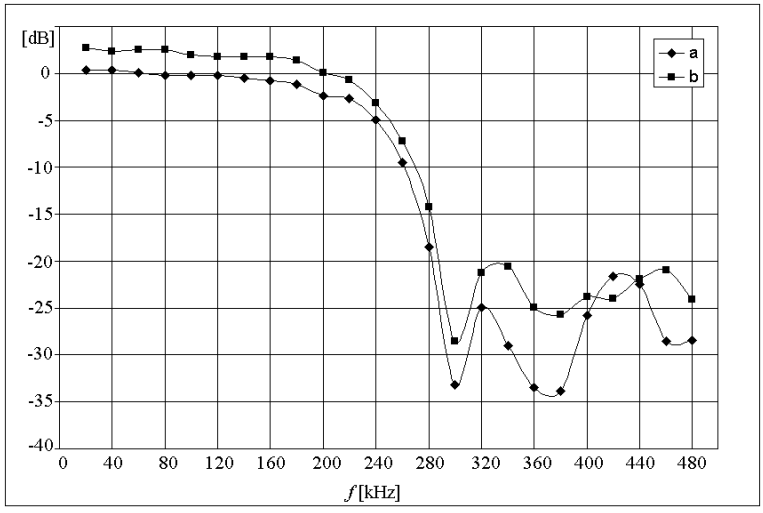


Figure 4.61: Frequency response of the second section: (a) of the structure with even-odd delay elements, (b) of the structure with Gillingham delay elements

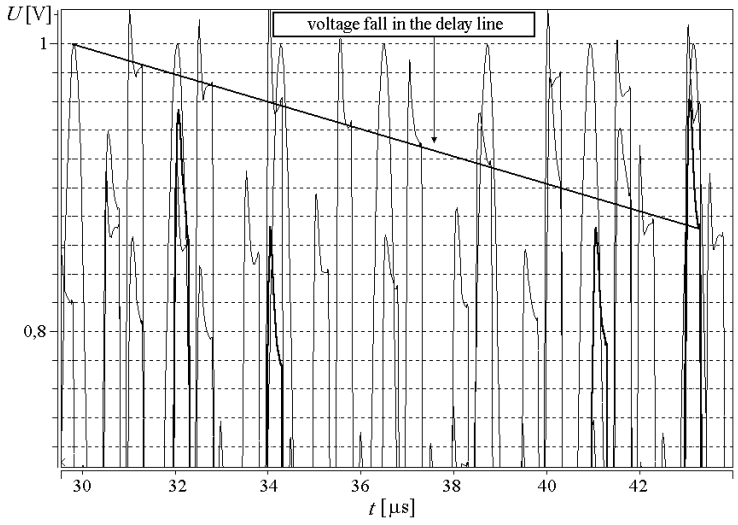


Figure 4.62: Voltage fall in a not optimized delay line

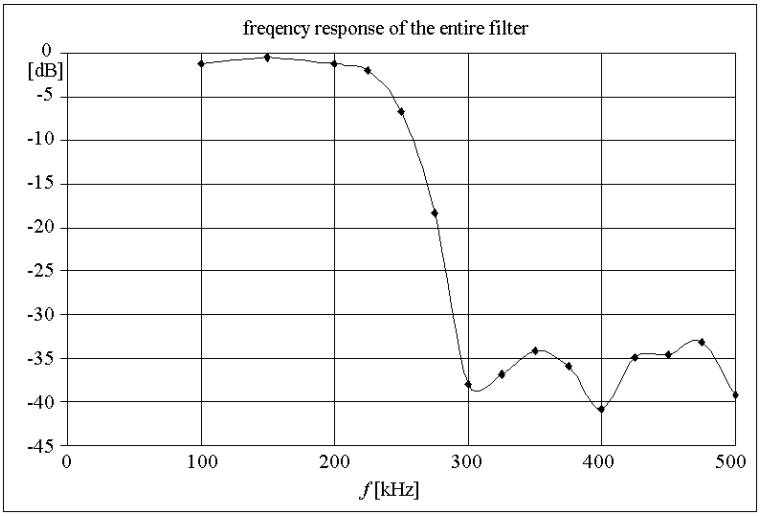


Figure 4.63: Frequency response of the even-odd delay line structure before optimization

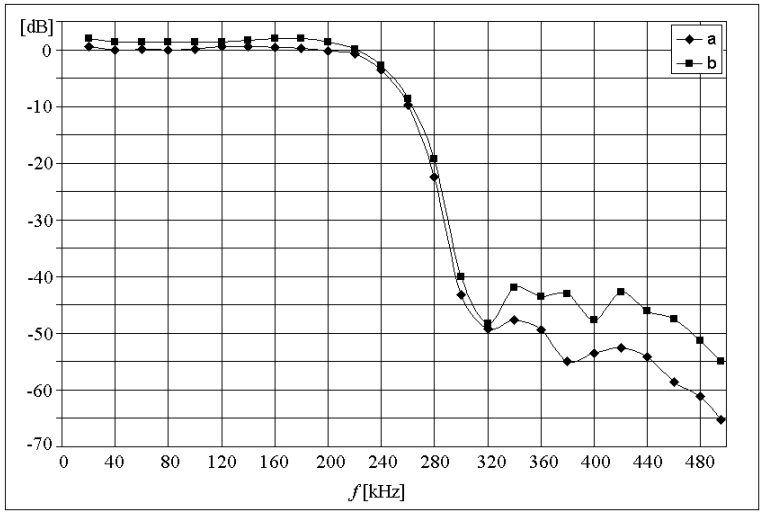


Figure 4.64: Frequency responses after optimization: (a) of the even-odd delay line structure, (b) of the Gillingham delay line structure

verifications we obtained a much better passband, as is illustrated in Figure 4.64. Both filters optimized in this way fulfill the initial requirements.

Above discussion shows that designers should be very careful with placing of elements and connections. A non optimal arrangement of connecting paths or other critical components can bring deterioration of the quality of a processed signal and of filtering properties.

During the research, which was carried out, the author gained experience about various SC FIR structures. Generally, the structure with even-odd delay elements behaves better than the structure with Gillingham delay elements. It results from the fact, that the filter with even-odd delay elements, realizing the same frequency response, consists less active elements than the filter with Gillingham delay elements. Thus, the samples are rewritten less times and the processing error is smaller. This aspect is really very significant for the quality of the stopband, since in the stopband the filter operates near the noise floor and every additional error means reduction of the attenuation.

4.5.2 Measurements of the chip

Clock system

In order to show the quality of the designed internal clock systems we present chosen waveforms. In Figure 4.65 waveforms of phases P1 and P2 of the internal clock system designed for the filter with Gillingham delay elements are plotted. In Figures 4.66, 4.67, 4.68, and 4.69 we present chosen pulses of the internal clock system of the even-odd SC FIR filter. These internal clock systems are driven with external 2 MHz clock generator realized using the AT90S1200 microcontroller. We can see that the clock

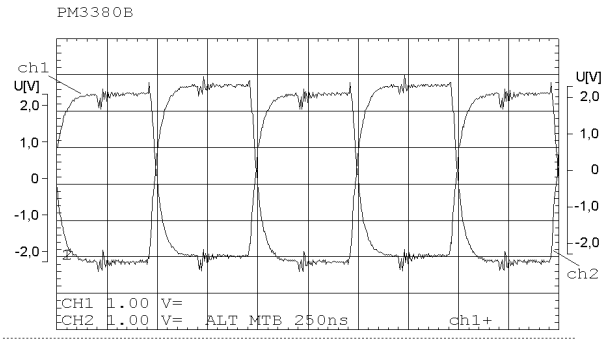


Figure 4.65: Clock phases P1 and P2 of the internal clock system of the Gillingham SC FIR filter

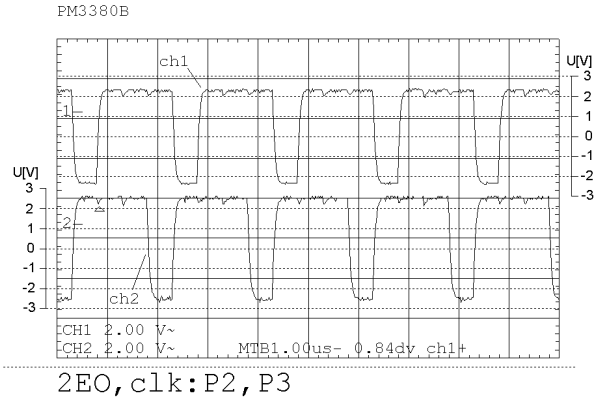


Figure 4.66: Clock phases P1 and P2 of the internal clock system of the even-odd SC FIR filter

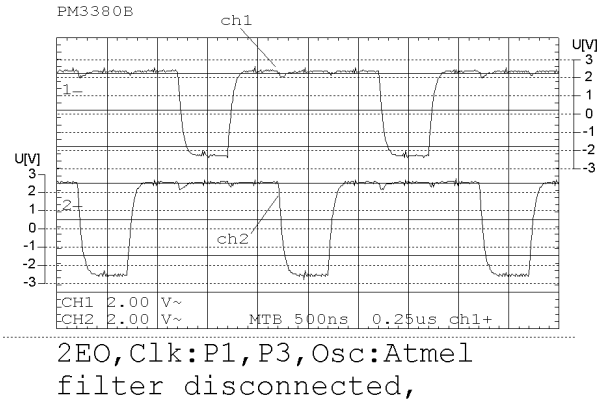


Figure 4.67: Clock phases P1 and P3 of the internal clock system of the even-odd SC FIR filter; clock system is disconnected from the filter structure

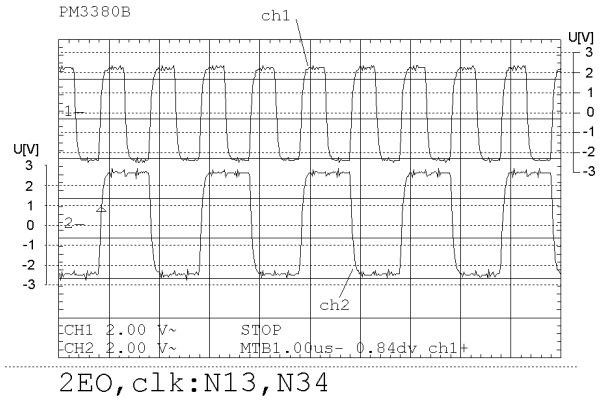


Figure 4.68: Clock phases N13 and N34 of the internal clock system of the even-odd SC FIR filter; clock system is disconnected fro the filter structure

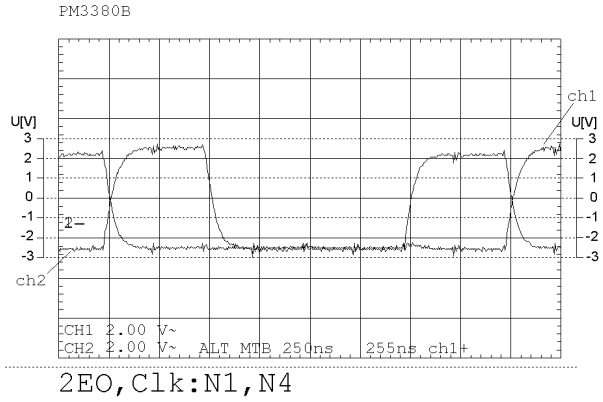


Figure 4.69: Clock phases N1 and N4 of the internal clock system of the even-odd SC FIR filter; clock system is disconnected from the filter structure

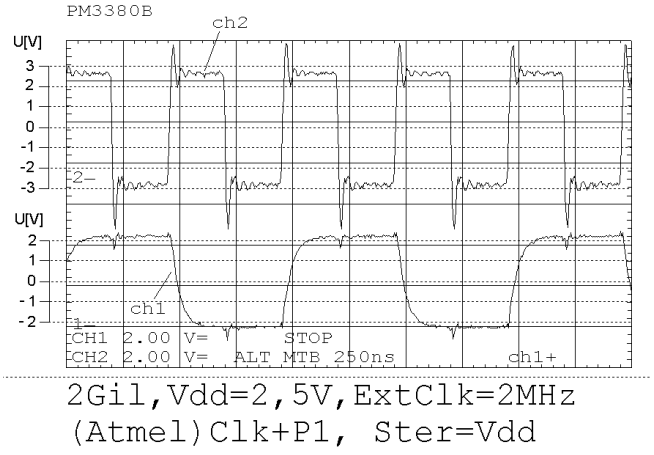


Figure 4.70: The control signal from the microcontroller and the phase P1 without compensation

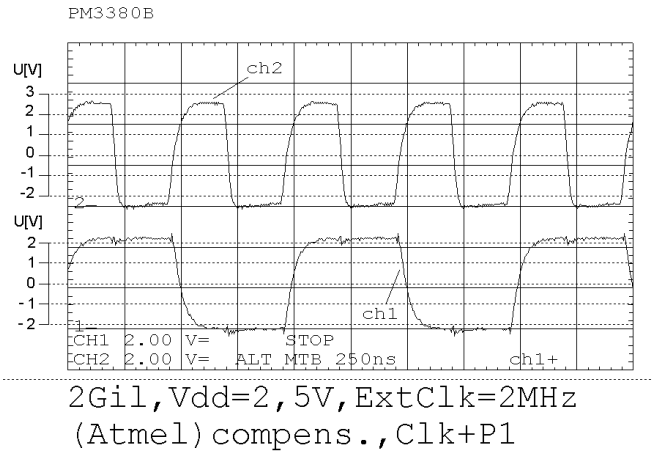


Figure 4.71: The control signal from the microcontroller and the phase P1 after compensation

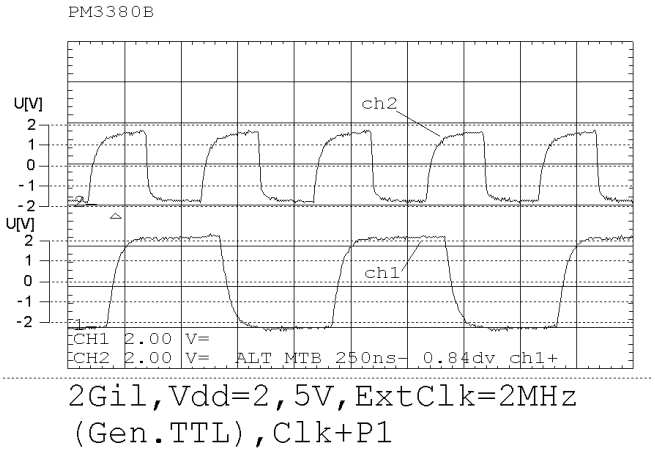


Figure 4.72: The control signal from the TTL output of the signal generator and the phase P1

impulses have correct shapes and cross each other near the zero voltage. The latter is a very important feature, which enables proper behavior of the filters.

Control clock pulses generated by the microcontroller can penetrate to the final clock pulses, especially if the microcontroller output circuit is not fully compensated (c.f., Fig. 4.70). Such a feedthrough negatively influences behavior of the whole filter structure. Thus, compensation of the microcontroller output circuit is necessary. After the compensation feedthrough is substantially decreased but not fully eliminated (c.f., Fog. 4.71). However, a fully satisfactory solution can be obtained using the TTL output of the signal generator (c.f., Fig. 4.72, in which the feedthrough is eliminated).

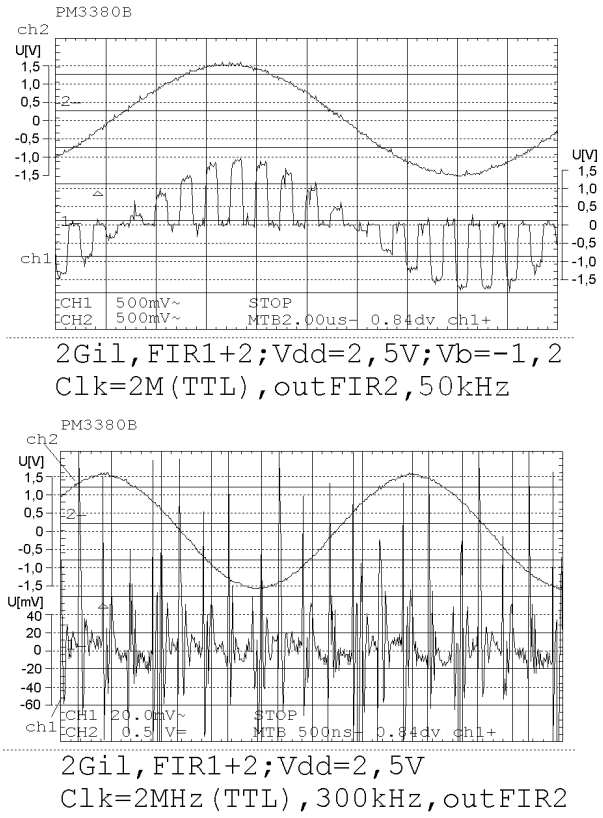


Figure 4.73: Input and output signal of the Gillingham SC FIR filter structure in: (a) the passband and, (b) the stopband

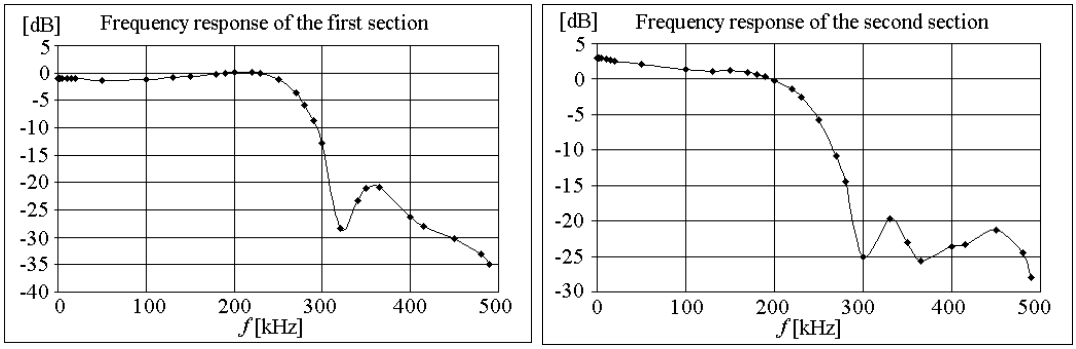


Figure 4.74: Frequency response of the first and the second section of the Gillingham SC FIR filter for $V_{\mathrm{DD}} = 2.5$ V and $V_{\mathrm{SS}} = -2.5$ V

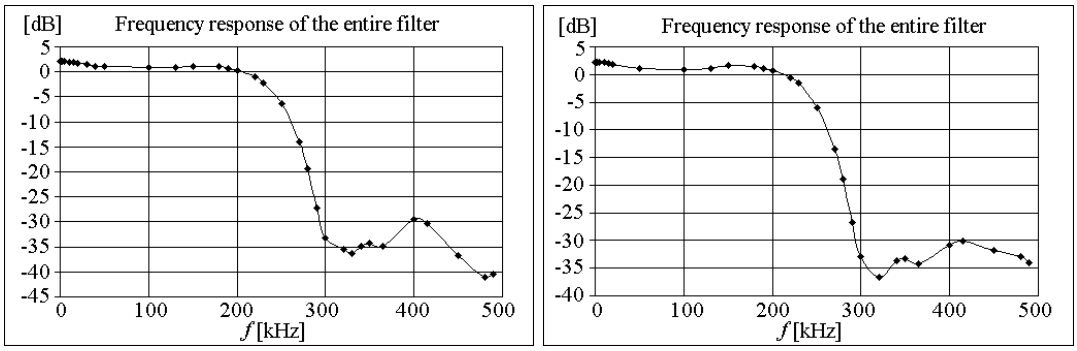


Figure 4.75: Frequency response of the Gillingham SC FIR filter for two sections connected in series: (a) for $V_{\mathrm{DD}} = 2.5$ V and $V_{\mathrm{SS}} = -2.5$ V, (b) for $V_{\mathrm{DD}} = 1.5$ V and $V_{\mathrm{SS}} = -1.5$ V

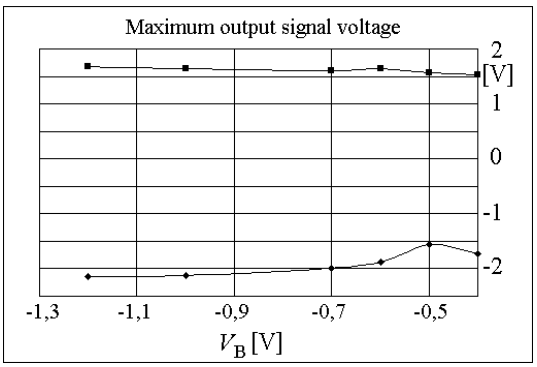


Figure 4.76: The maximum value of the non distorted signal as a function of the bias voltage V_{B} in the Gillingham SC FIR filter

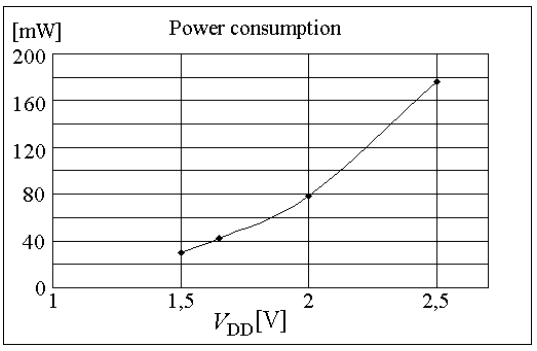


Figure 4.77: Power consumption (together with the clock system) as a function of the supply voltage in the Gillingham SC FIR filter

Measurements of the Gillingham SC FIR filter

In Figure 4.73 we present waveforms of the input and the output signal of the Gillingham SC FIR filter structure. In Figure 4.74 we present the frequency responses of the first and the second section of the filter. The supply voltages are: $V_{DD} = 2.5$ V and $V_{SS} = -2.5$ V.

Results for the lover value of the voltage supply e.g. $V_{DD} = 1.5$ V and $V_{SS} = -1.5$ V are similar (c.f., Fig. 4.75).

The next step was measurement of the entire filer (both sections connected in series). The measured frequency responses are presented in Figure 4.75. They are slightly worse than those obtained in the HSPICE simulations but nevertheless they are acceptable. The main reason for this discrepancy is inaccuracy of the measurement environment. It is difficult to fully compensate all inaccuracies in the analog circuits and SC FIR filters are very sensitive to such elements.

At the end of this part of measurements the power consumption of the structure was evaluated as a function of the supply voltage. Decreasing of the value of the supply voltage from 5 to 3 V resulted in some degradation of the stopband attenuation. This is somehow disadvantageous, but in the same time the power consumption is strongly reduced (about 5.5 times). This is in turn a very important advantage in applications, in which this parameter is critical (e.g., mobile phones) [35, 41]. Power consumption as a function of the supply voltage is presented in Figure 4.77.

Additionally we have measured the maximum value of a non distorted signal as a function of the bias voltage V_B (Fig. 4.76). This influence is much milder than that in the first prototype (Fig. 4.47). In the first prototype the bias voltage strongly influences the value of a non distorted signal, because in this case V_B controls the output stage of the OA.

In the first prototype the value of V_B has a strong influence also on the power consumption (Fig. 4.45). Furthermore, in the first prototype the optimum value of of V_B for a non distorted signal differs from the optimum value for the low power consumption. Power consumption is minimized for the lowest value of V_B but the signal quality is the best for the highest value of V_B. In the second prototype this severe problem has been eliminated.

Measurements of the even-odd SC FIR filter

Measurements similar to those of the Gillingham SC FIR filter were performed also for the even-odd SC FIR filter. In Figure 4.78 the signal waveforms in the passband and in the stopband are presented. Frequency response for the supply voltages $V_{DD} = 2.5$ V and $V_{SS} = -2.5$ V are presented in Figure 4.79 (sections measured separately) and in Figure 4.80 (sections connected in series). The obtained curves fulfill all requirements.

It is worth noting that the power consumption is in the even-odd SC FIR filter lower than that in the Gillingham SC FIR filter (Fig. 4.82). This results from the lower

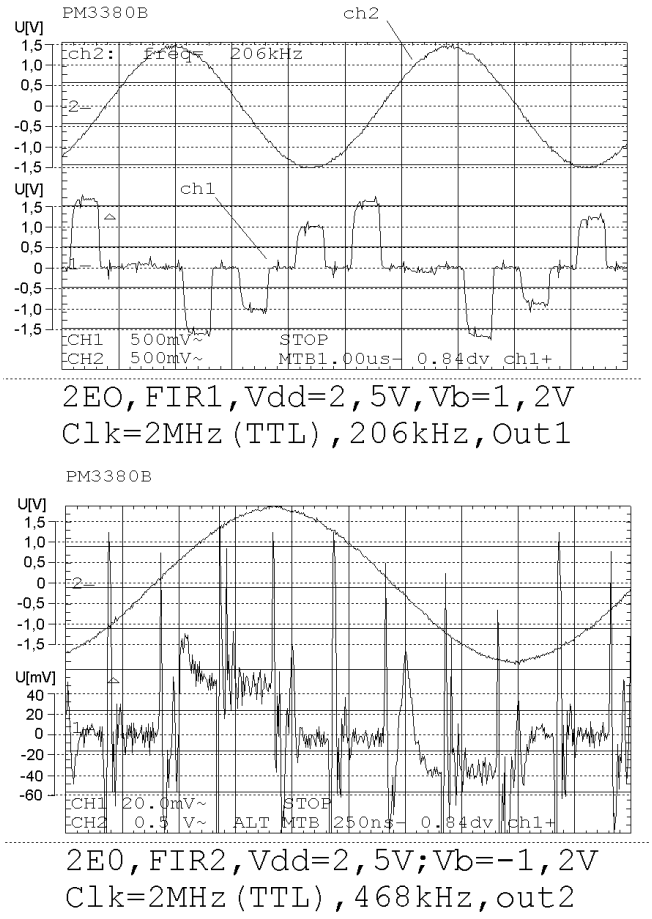


Figure 4.78: Waveforms of the input and the output signals of the even-odd SC FIR filter in: (a) the passband and, (b) the stopband

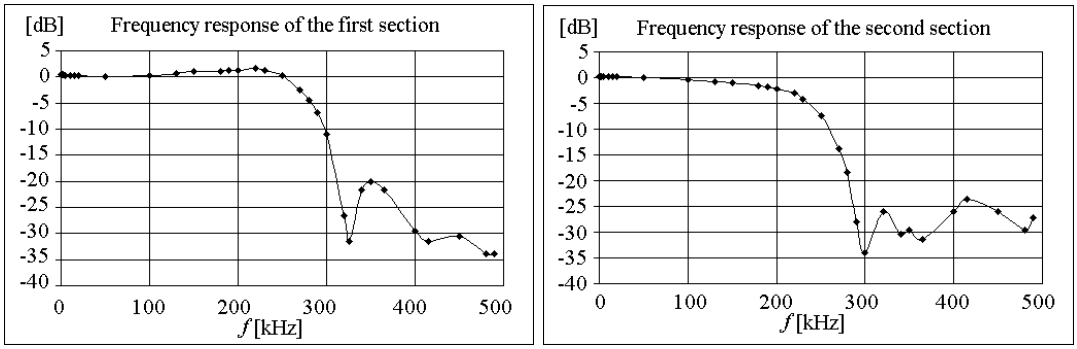


Figure 4.79: Frequency response of the first and the second section of the even-odd SC FIR filter for $V_{DD} = 2.5$ V and $V_{SS} = -2.5$ V

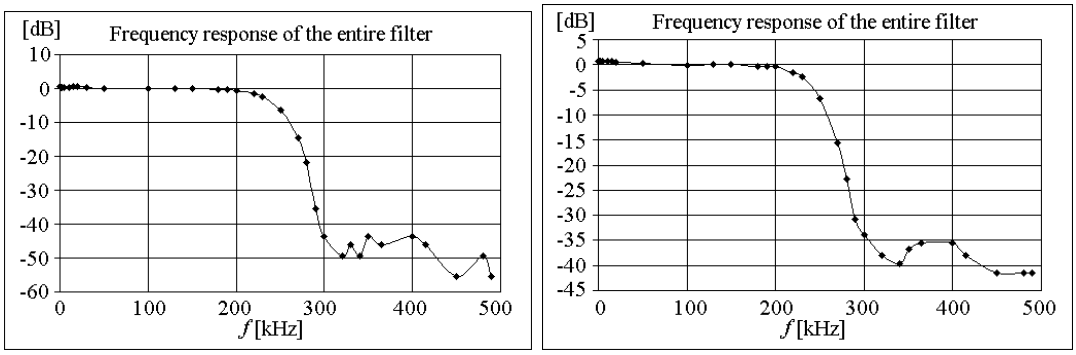


Figure 4.80: Frequency response of the even-odd SC FIR filter for two sections connected in series for: (a) $V_{\mathrm{DD}} = 2.5$ V and $V_{\mathrm{SS}} = -2.5$ V, (b) $V_{\mathrm{DD}} = 1.5$ V and $V_{\mathrm{SS}} = -1.5$ V

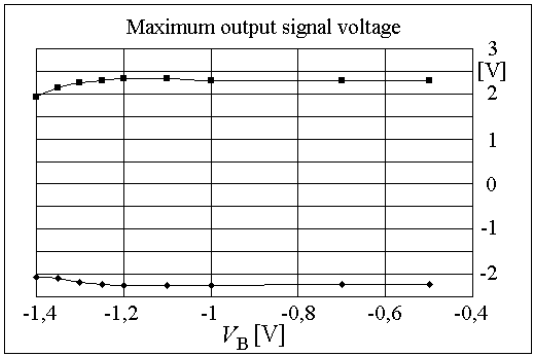


Figure 4.81: The maximum value of the not distorted signal as a function of the bias voltage V_{B} for the even-odd SC FIR filter

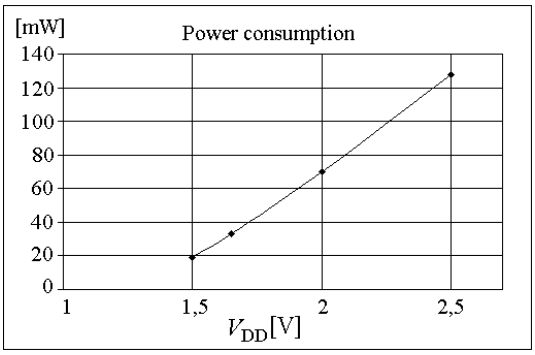


Figure 4.82: Power consumption (together with the clock system) as a function of the supply voltage for the even-odd SC FIR filter

number of OA's in the even-odd SC FIR filter. Higher is also a ratio (now equal to 8 times) of the power consumption reduction, i.e., this with higher supply voltages $V_{DD} - V_{SS} = 5$ V to that with lower supply voltages $V_{DD} - V_{SS} = 3$ V. The minimum value of the power consumption is equal to 16 mW.

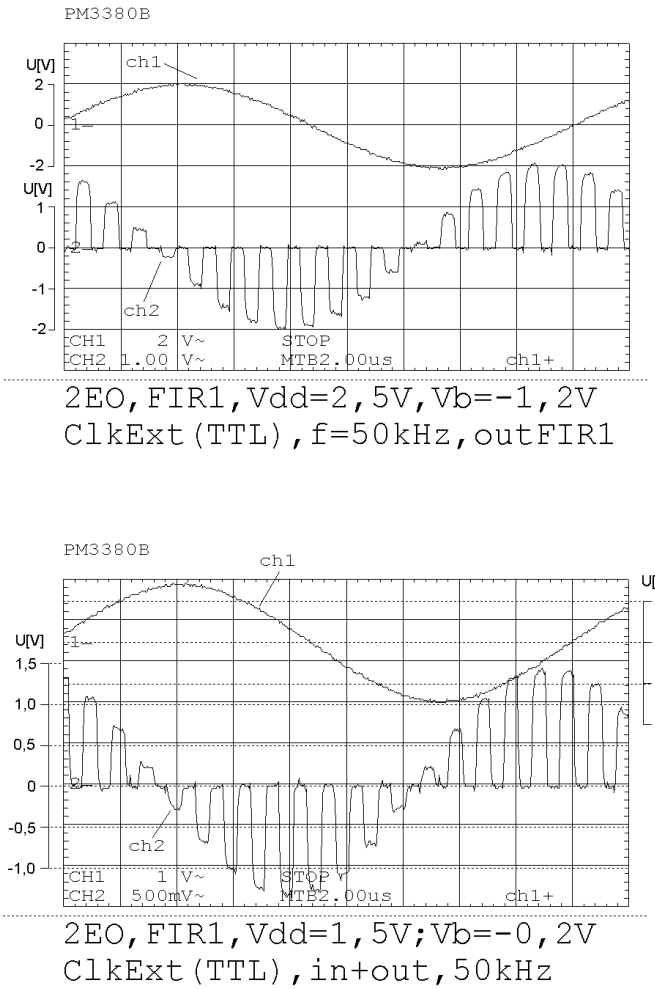


Figure 4.83: Waveforms the maximum non distorted output signals (the lower curves) of the even-odd SC FIR filter in the case of the voltage supply 5 V (top) and 3 V (bottom)

Furthermore, in the even-odd SC FIR filter values of the non distorted output signal are higher than those in the Gillingham filter. This is illustrated in Figure 4.81, which shows amplitude of the non distorted output signal as a function of the bias voltage V_B. In Figure 4.83 waveforms of the maximum non distorted output signal are plotted for supply voltages $V_{DD} - V_{SS} = 5$ V and $V_{DD} - V_{SS} = 3$ V.

4.6 Measurement environment

Measurements were performed using of the following laboratory equipment:

- Measure modul which consists of the: Power supply, Signal Conditioner, External clock generator based on the microcontroller ATMEL,
- Measurement environment for the chips which contains: Signal generator MAX-COM MX-2020, Function generator G432 Analog osciloscope HUNG-CHANG 3502C 20MHz, Digital osciloscope FLUKE PM2280B 100 MHz, 10 GS/s with RS connection to the PC computer [14], Signal generator METEX MS-9150 and Digital multimeter ESCORT 97.

The constructed power supply consists of three galvanicly separated segments:

- First segment is the power supply, which delivers 5 V voltage for the supply of the microcontroller. This circuit is built on the basis of the IC voltage regulator 7805, with the separated digital ground connection.
- Second segment consists of two independent supplies, connected to the some rectifier. First of them delivers a voltage in the range of 1.25 V to 2.5 V (DC component in the voltage summer, the level of the analog ground). The second one delivers a voltage in the range of 2.5 V to 5 V (V_{DD} voltage supply for tested chips). Both supplies have identical construction and are based on the precise IC voltage regulator LM 317T.
- Third segment consists of two supplies working in the symmetric differential configuration with a possibility of independent voltages for control in both branches. The positive voltage is produced by the IC voltage regulator LM 317T and the negative voltage is produced by the IC voltage regulator LM 337T. These circuits supply the OAs in the Signal Conditioner. From the positive voltage the (V_{B}) is obtained in the range of 1 V to 5 V, with the use of the voltage divider. This voltage is used as a bias voltage for polarization of the OA's in the chips.

The Signal Conditioner is built on the basis of the TL-081 operational amplifier. This circuit adds two voltages: one is the signal delivered from the external function generator (in tests the MX 2020 MAXCOM generator was used), the second one is the DC voltage from the voltage supply. The resulting signal is delivered to the inverting amplifier built on the basis of TL-081 OA. The Signal Conditioner adjusts signal levels and protects measured chips.

Integrated circuits were fabricated in cooperation with EUROPRACTICE. The first prototype is encapsulated in the CQFP64 package, and is placed directly on the testing board.

The second prototype is encapsulated in the PGA100 package (Fig. 4.84), and is placed on the additional board (Fig. 4.85a, b), which is separated from the testing

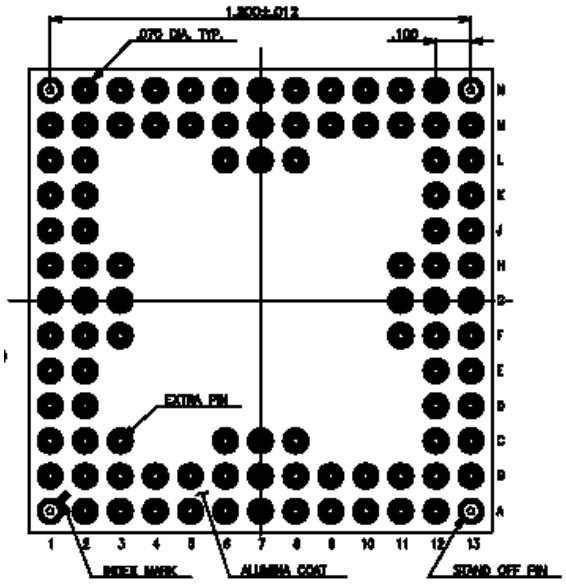


Figure 4.84: PGA 100 package

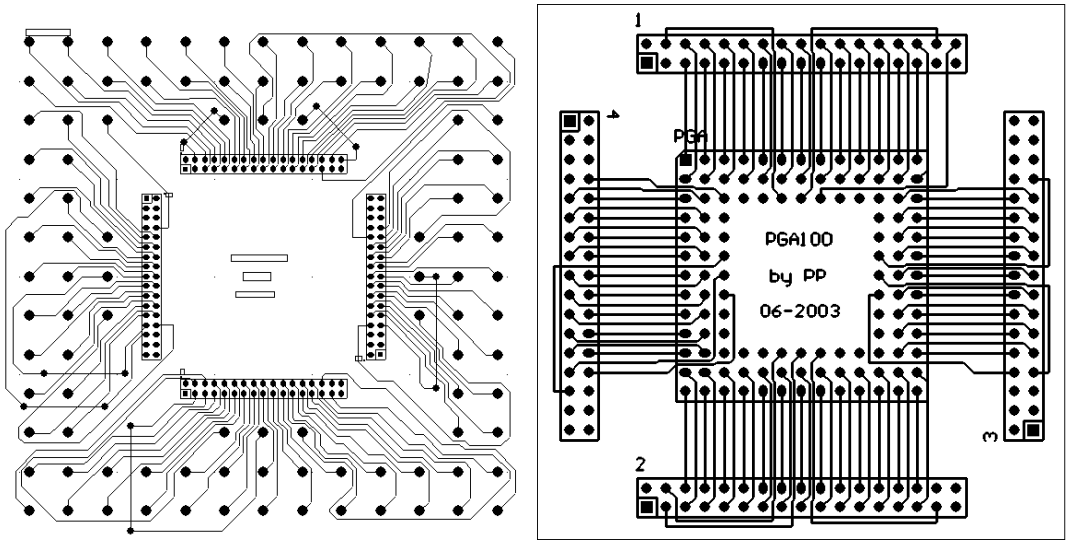


Figure 4.85: Connection boards : (a) base board, (b) doughter board

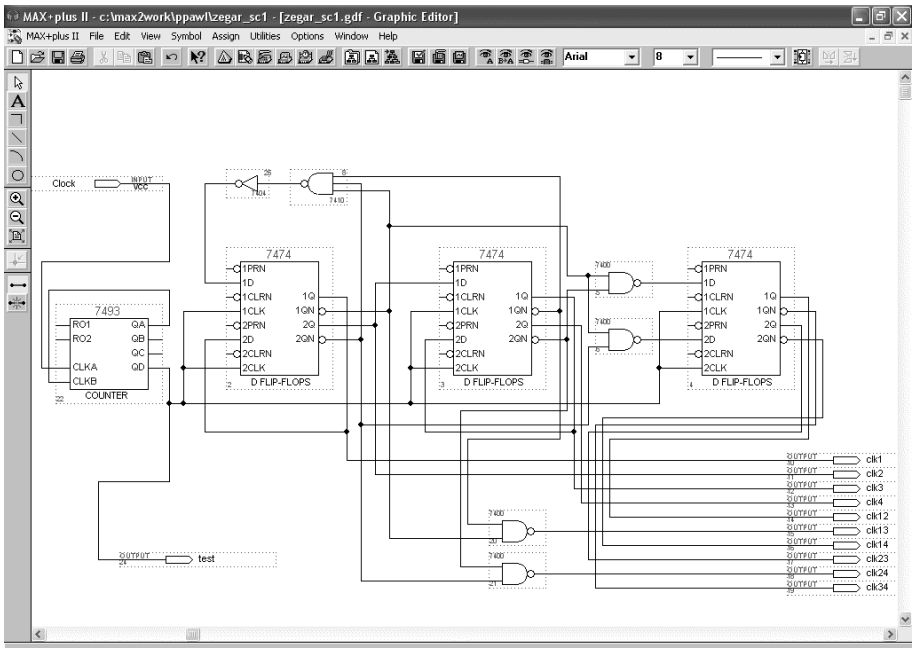


Figure 4.86: External clock system for the even-odd SC FIR filter designed in the MAX + plus II environment

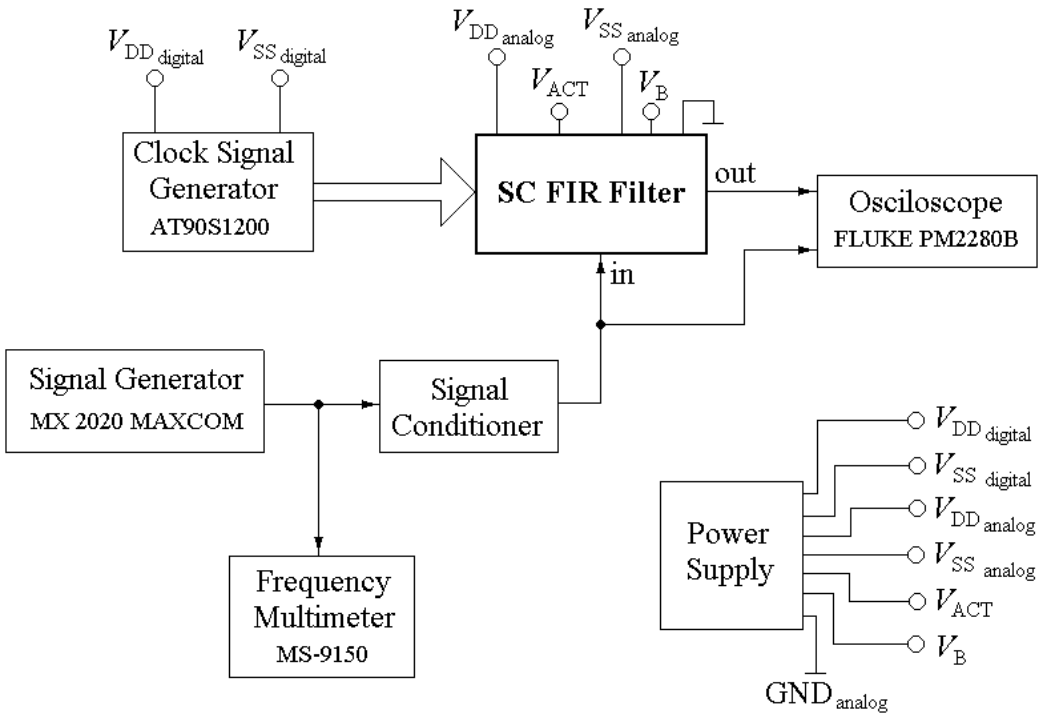


Figure 4.87: Block diagram of the measurement environment

board to avoid feedthroughs from the external clock system, which is placed on the testing board. Connection with the testing board is realized by the shielded cables.

The even-odd SC FIR filter needs much more complicated clock system (20 different clock signals) than the Gillingham SC FIR filter. This creates a problem in the case of the external clock system. Since the ATMEL microcontroller is insufficient, we have used the Altera FPGA to this purpose. In Figure 4.86 the design of the clock system in the MAX + plus II environment is presented. This clock system was implemented in the EPF10K70 Chip [58, 59].

The internal clock systems and the clock system realized externally in the FPGA are driven by the AT90S1200 microcontroller or by the signal generator METEX MS-9150 (TTL output).

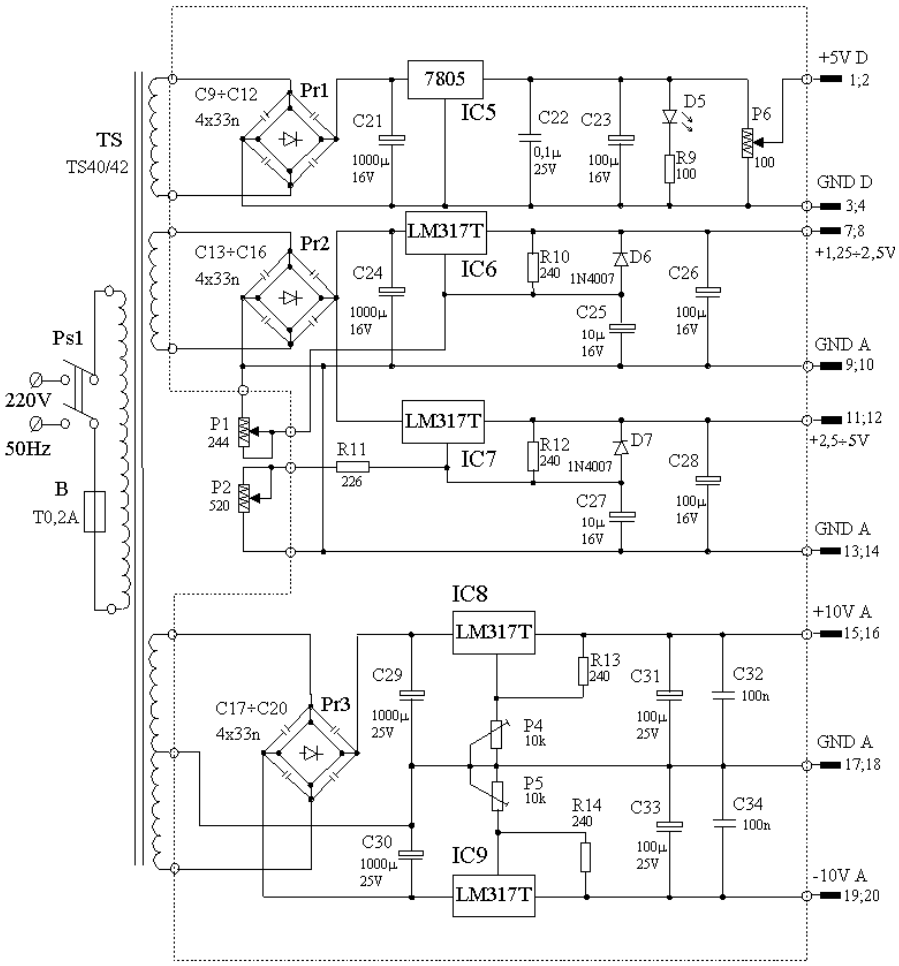


Figure 4.88: Power supply scheme

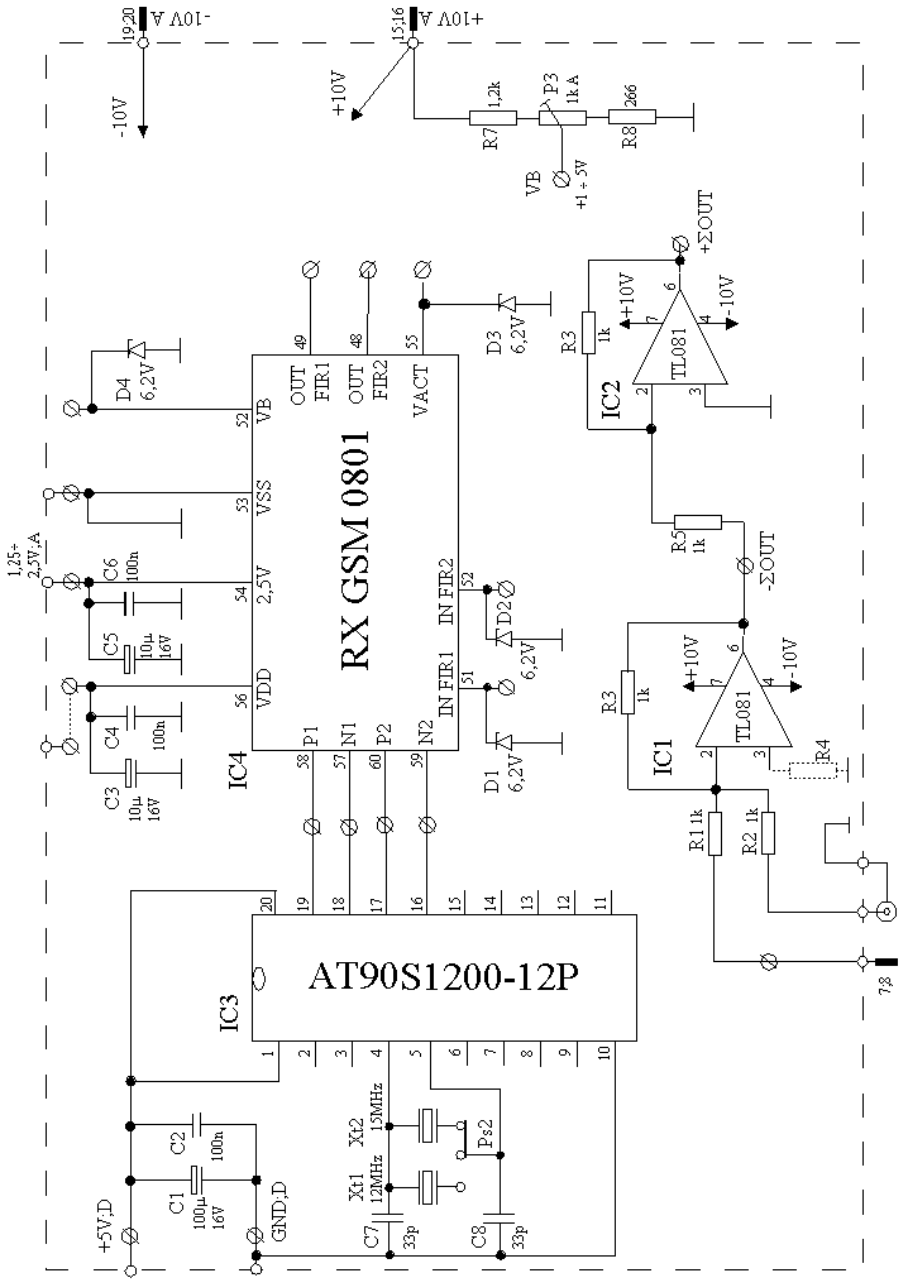


Figure 4.89: Measurement environment of the RX GSM 0801 chip

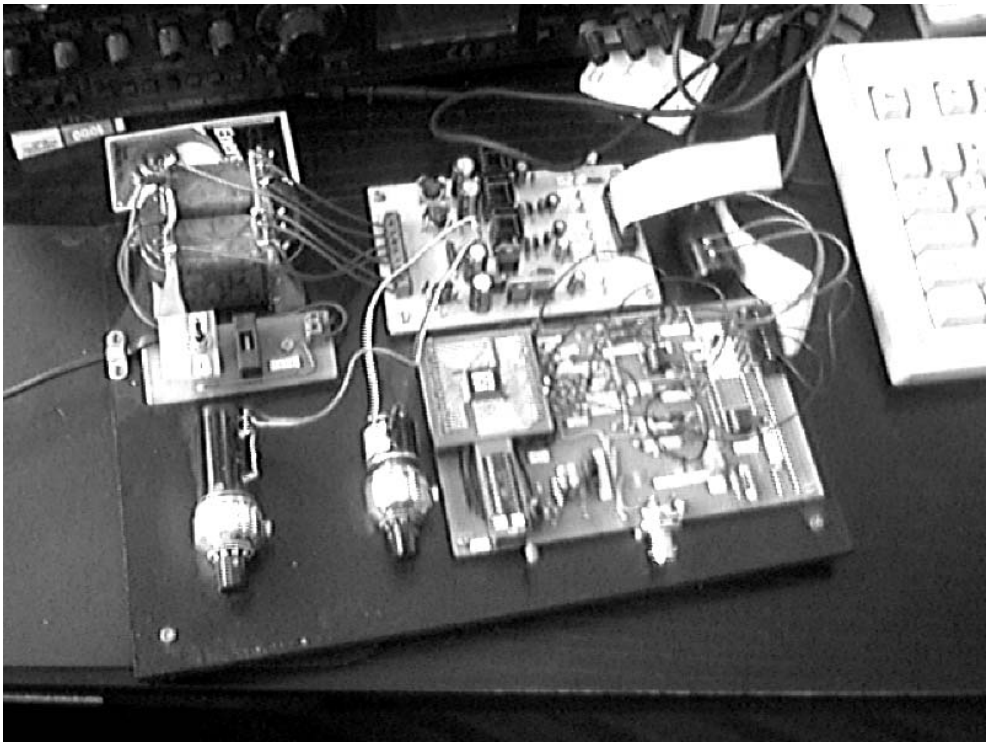


Figure 4.90: Testing board for RX GSM 0801

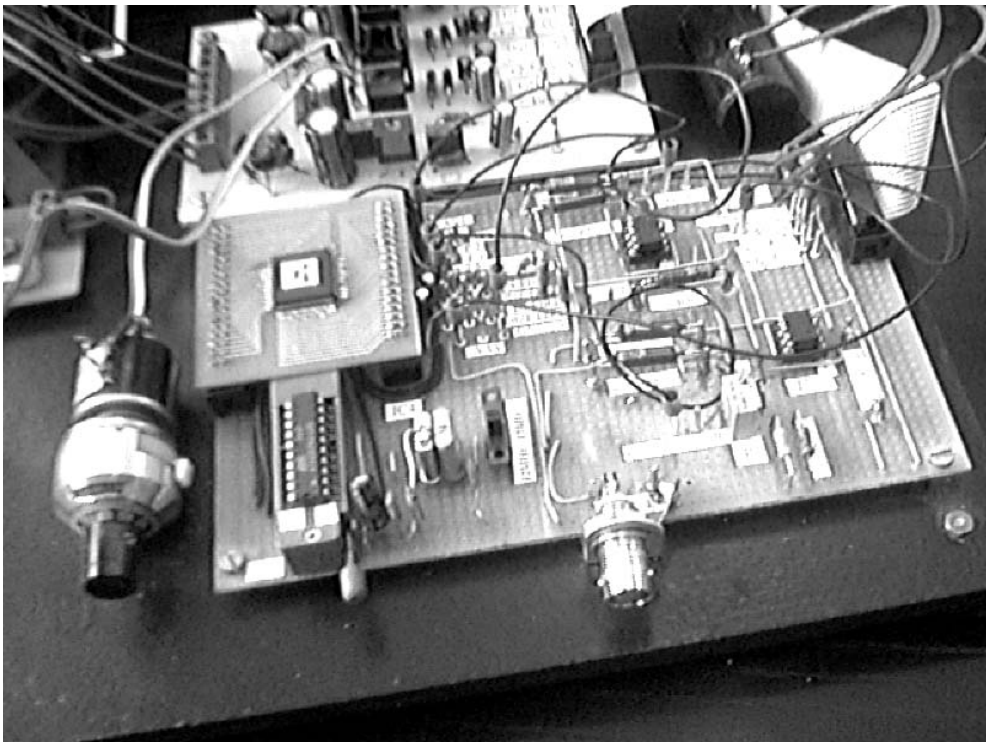


Figure 4.91: Configuration board and the clock circuit

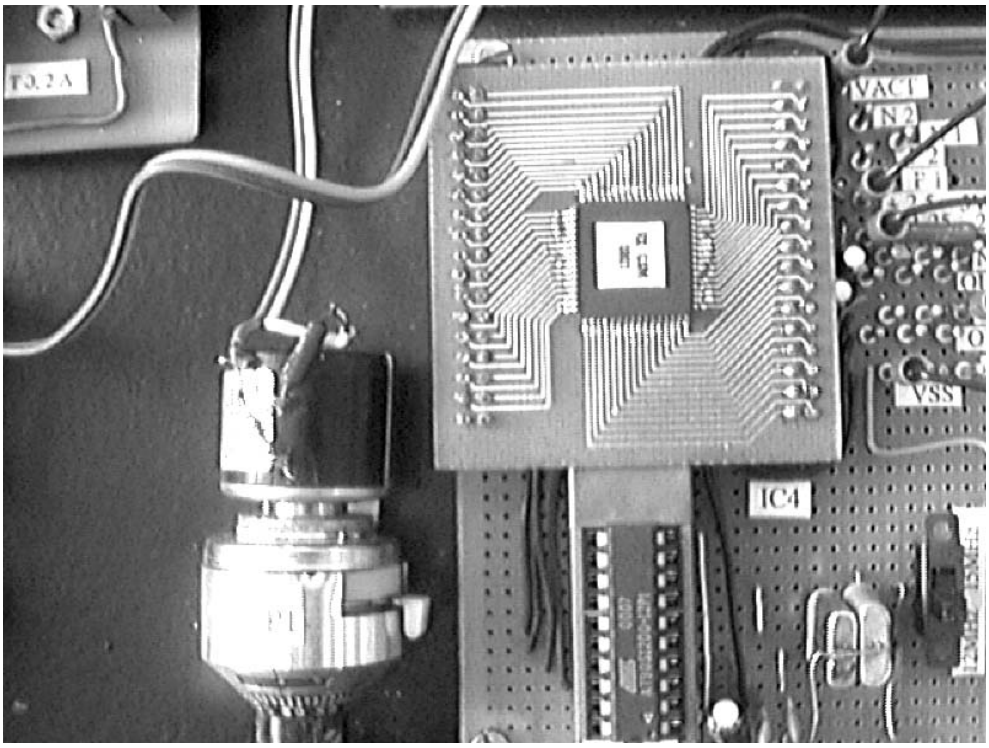


Figure 4.92: RX GSM 0801 chip (upper block). Programmable Atmel microcontroller (bellow)

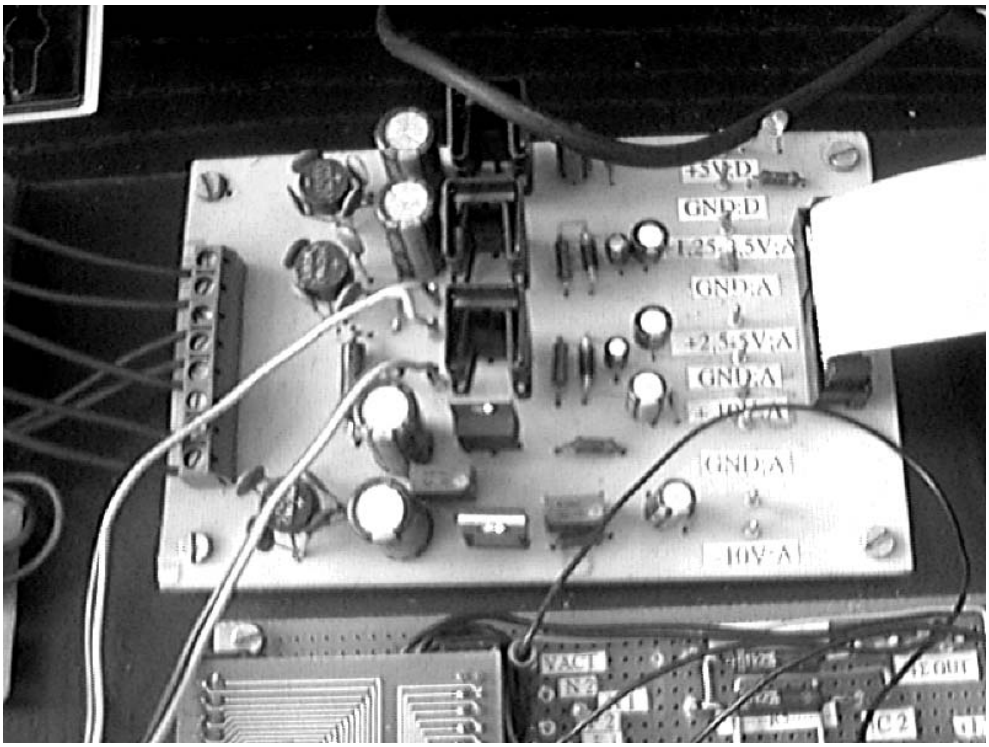


Figure 4.93: Board with the power supply circuits

Chapter 5

Conclusions

The scientific aim of this Ph. D. Dissertation, formulated in Section 1.2, was realized in several stages.

The first stage consisted in the theoretical comparison of various SC FIR filter structures. The following criteria were used for this comparison:

- integrated circuit area,
- power consumption,
- quality of the processed signal,
- clock system complexity.

Investigations at this stage were necessitated by several reasons. Lack of economical means made it impossible to design, realize, and verify all possible SC FIR filter structures. Thus, those omitted might be verified in future.

It was necessary to choose two or three potentially best structures for further realization. The choice had been made in such a way as to enable the technical realization of the chosen filter structures. Their analysis, design, and measurements should deliver universal results, allowing objective assessment of a wide class of circuits. This aim was achieved. The structures chosen for the realization proved to be the best in view of the assessment criteria mentioned above.

The theoretical analysis proved to be essential also for that reason that it showed inadequacy of the simplest method of assessing the filter structures area, i.e., the method, which does not take into consideration frequency response realized by a designed circuit. It turned out that the estimated values of area of the basic elements (e.g., capacitors, switches, OA's) should not be uncritically taken into consideration. Values of these elements of coefficient capacitors, depend on numerous factors, like the mentioned above frequency response, the type of structure, and position of the given element within this structure. The most important for the circuit area estimation is the type of the filter frequency response, and more precisely the filter coefficient values. What is essential

here is not so much the maximum absolute value of the coefficients in the filter transfer function as the spread between the smallest and the largest coefficient (up to their absolute values).

The smallest coefficient in the circuit is represented by a capacitor, the capacitance of which is the same as the capacitance of the so called unit capacitor. This fact indicates that if the spread between coefficients is wide big, then the maximum capacitance and consequently capacitors area can be large enough to make a practical realization of such circuit impossible. This conclusion has become a starting point for further investigations.

At the second stage of the carried out research, my main concern was a method, which might be helpful in solving of the problem mentioned above. The only way to achieve this purpose consists in reducing the chip area of the coefficient capacitors with the frequency response of the filter unchanged. This objective has been achieved by dividing the basic filter into smaller sections connected in series (or more precisely in cascade). The product of all of the partial transfer functions gives the overall transfer function of the designed filter. The transfer functions of particular sections are chosen in such a way as to minimize the coefficient spread in each of these sections. In consequence the total chip area of all capacitors is much smaller than in the case of the structure, which has not been divided.

In the extreme case (i.e., many simple sections) the chip area may again be unrealistic, as the exactness requirements are becoming severe for each of these sections and this can only be achieved with larger capacitances. Thus the smallest capacitance must be realized as a parallel connection of many unit capacitors.

The most important advantage of the proposed method is not only the possibility to calculate the chip area in a more accurate way, but also the possibility to realize such filters, which were not feasible in a direct approach (structure not divided). This method proved indispensable in this part of investigation, which dealt with practical realization of the SC FIR filters. It must be stressed that without this method practical realization of the filters would be impossible and that because of a very high chip area and, in consequence, high costs of production.

To illustrate these considerations a carefully selected application, namely the design of the channel filter for the GSM receiver has been chosen. In case of the direct realization the total chip area would be ca. six times higher and the cost would explode.

The next research stage was to solve the problem of the design of the clock systems for control of the SC FIR filter structures. SC FIR filters in many cases require complicated multiphase clock systems. Apart from this, in many filter structures particular switches are driven by more than one clock phase. This generates problems with the clock phase separation. Many solutions of this problem have been proposed. These were partially implemented in the second prototype in the case of the even-odd delay line structure. The significance of these methods is particularly visible in the case of structures driven by an external clock system. If the number of the IC pins is limited, then the filters with high order N in many structures may be unfeasible, because of a great number

of the clock phases. In such cases minimization of the number of the clock phases is very important.

In the course of investigations a family of new even-odd filter structures was proposed. The innovation consists in increasing the delay element order. Owing to this, it is possible to store a greater number of the signal samples in a single delay element. In result, filter with a given order N can be realized using the lower number of the delay elements, and in consequence, the lower number of OA's. The number of OA's is proportional to the power consumption. The disadvantage of this can be the extension of the chip area. Whether or not the mentioned extension occurs and if so to what degree depends on the frequency response of the filter. In the dissertation the analysis has been made of the chip area in different cases of the frequency responses and different orders of the even and odd delay elements. It turns out that it is necessary to analyze each case separately searching for a compromise between different conflicting parameters.

One of the most important stages of my research referring to this Ph.D. dissertation was practical verification of the theoretical considerations shortly characterized and recapitulated above. Within the compass of several years two prototype integrated circuits were constructed, which implement some of the filter structures.

In the first prototype integrated circuit the small number of the accessible pins and the small area made it necessary to choose the structure with the clock system of the least possible complexity and the smallest possible area. The only filter satisfying these requirements is the Gillingham delay line structure.

This filter was optimized and corrected and was incorporated into the second prototype. The comparison of the results presented in Figs. 4.43 and 4.74 shows the improvement of the results in the stopband of the second prototype. This improvement is the effect of – among other things – the compensation of parasitic capacities in the delay line of the second prototype. The OA was also improved. In the second prototype solutions of the greater complexity were applied.

Apart from the filter, which was constructed on the basis of the Gillingham structure, there was implemented also the even-odd delay line structure and internal prototype clock systems.

The correct measurement verification of the structures operational in controlling these systems has shown that in subsequent designs external clock systems can, in principle, be eliminated.

The results of the measurements proved very good, especially for even-odd delay line structures — what was to be expected. This structure has a shorter delay line, that is with a smaller number of operational amplifiers. This results in smaller power consumption. The shorter delay line also means a smaller number of rewriting of the signal samples and this, in turn, diminishes the error connected with rewriting. The measurements show this very clearly.

To sum up, I can most certainly say that the obtained measurements allow for a positive assessment of the work as a whole, of both its theoretical and practical parts. Thus, assumed aims have been achieved and the scientific thesis has been proved.

The author hopes that this work makes a good basis for further investigations in this field.

Bibliography

[1] A. Dąbrowski, *Multirate and multiphase switched - capacitors circuits*, Chapman & Hall, London., 1997

[2] A. Dąbrowski, U. Menzi, G.S.Moschytz, Design of switched-capacitor FIR filters with application to a low-power MFSK receiver, *IEE Proceedings-G*, Vol. 139, No. 4, August 1992, pp. 450–466.

[3] A. Dąbrowski, U. Menzi, G.S. Moschytz, Offset-compensated switched-capacitor delay circuit that is insensitive to stray capacitance and to capacitor mismatch, *Electr. Lett.*, 1989, Vol. 25, No. 10, pp. 623–624, No. 6, 1989, pp. 387–389.

[4] A. Dąbrowski(red.), *Przetwarzanie sygnałów przy użyciu procesorów sygnałowych*, Wydawnictwo Politechniki Poznańskiej, Poznań 1998 (in Polish)

[5] R. Gregorian, G. C. Temes, *Analog MOS integrated circuits for signal processing*, John Wiley & Sons, New York 1985.

[6] P.P. Vaidynathan *Multirate systems and filter banks*, Prentice-Hall, Englewood Cliffs, 1993

[7] David A. Johns, Ken Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, New York, Inc., 1997,

[8] Amar Mukherjee, *Introduction to nMOS and CMOS VLSI Systems Design*, Prentice-Hall, New Jersey, 1986.

[9] Z. Ciota, *Theory and practical realization of analog integrated filters particularly taking into account finite impulse response filters*, Łódź University of Technology Press, Łódź 1996 (in Polish)

[10] D.C. Grünigen, *Entwurfs- und Analyseverfahren für Filter mit geschalteten Kondensatoren*, ETH Zurich, Institut für Signal und Informationsverarbeitung, Zurich 1983

[11] Behzad Razavi, *Principles of Data Conversion System Design*, The Institute of Electrical and Electronics Engineers, Inc., New York, IEEE Press

[12] Z. Nosal, J. Baranowski, *Układy elektroniczne cz. I. Układy analogowe liniowe*, WNT Warszawa 1994 (in Polish)

[13] J.Baranowski, B.Kalinowski, Z.Nosal, *Układy elektroniczne cz. III, Układy i systemy cyfrowe*, WNT Warszawa 1994 (in Polish)

[14] W. Nawrocki, *Komputerowe systemy pomiarowe*, WKiŁ, Warszawa 2002 (in Polish)

[15] A.Napieralski, M.Napieralska, M.Grecki, *Computer laboratory for CAD of power and integrated circuits, Computer-aided design and computer-aided engineering in electronic engineering education*, Warsaw University of Technology 1996

[16] Samuel D. Stearns, Ruth A.David, *Signal processing algorithms in Matlab*, Prentice Hall P T R, Upper Saddle River, New Jersey 07458

[17] G.S. Moschytz, The morphological approach to network and circuit design, *IEEE Trans. Circuits Syst.*, Vol. CAS-23, No. 4, 1976, pp. 239–242

[18] A. Petraglia, S. K. Mitra, Effects of Coefficient Inaccuracy in Switched-Capacitor Transversal Filters, *IEEE Trans. Circuits Syst.*, Vol. 38, No. 9, Sep. 1991, pp. 977–983

[19] G. Fischer, Analog FIR filters by switched-capacitor techniques, *IEEE Trans. Circuits Syst.*, vol. CAS-37, No. 6, 1990, pp. 808–814.

[20] Z. Ciota, A. Napieralski and J. L. Noullet, Analog interpolated finite impulse response filters, *Proc. European Conf. Circuit Theory Design*, Davos, Switzerland, 1993, pp. 1367–1372

[21] J.E. Franca, Non-recursive polyphase switched-capacitor decimators and interpolators, *IEEE Trans. Circuits and Systems*, 1985, CAS-32 (9), pp. 877–887

[22] J. E. Franca and S. Santos, FIR switched-capacitor decimators with active-delayed block polyphase structures, *IEEE Trans. Circuits Syst.*, Vol. CAS-35, No. 8, 1988, pp. 1033–1037

[23] B.G. Pain, Alternative aproach to the design of switched-capacitor filters, *Electron. Lett.*, 1979, 15 (14), pp. 438–439

[24] J.J. Mulawka, Switched-capacitor analogue delays comprising unity gain buffers, *Electron. Lett.*, 1981, 17 (7), pp. 276–277

[25] K. Nagaraj, Switched-capacitor delay circuit that is insensitive to capacitor mismatch and stray capacitance, *Electron. Lett.*, 1984, 20 (16), pp. 663–664

[26] T. Enomoto, T. Ishihara, M.A. Yasumoto, Integrated tapped MOS analogue delay line using switched capacitor technique, *Electron. Lett.*, 1982, 18 (5), pp. 193–194

[27] P. Gillingham, Stray-free switched-capacitor unit-delay circuit, *Electron. Lett.*, 1984, 20 (7), pp. 308–310

[28] A.E. Said, Stray-free switched-capacitor building block that realizes delay, constant multiplier, or summer circuit, *Electron. Lett.*, 1985, 21 (4), pp. 167–168

[29] V.F. Dias, J.E. Franca, Parasitic-compensated switched-capacitor delay lines, *Electron. Lett.*, 1988, 24 (7), pp. 377–379

[30] Y.S. Lee, K.W. Martin, A switched-capacitor realization of multiple FIR filters on a single chip, *IEEE J. Solid State Circuits*, SC–23 (4), 536–542

[31] Eugene B. Hogenauer, An Economical Class of Digital Filters for Decimation and Interpolation, *IEEE Transaction on Acoustic, Speech, and Signal Processing*, Vol. ASSP-29, No. 2, April 1981

[32] David J. Goodman, Michael J. Carey, Nine Digital Filters for Decima tion and Interpolation, *IEEE Transaction on Acoustic, Speech, and Signal Processing*, Vol. ASSP-25, No. 2, April 1977

[33] A. Dąbrowski, R. Długosz, Chip area estimation for SC FIR filter structures in CMOS technology, in *Mixed Design of Integrated Circuits and Systems*, Kluwer, Boston 1998, pp. 143–148.

[34] A. Dąbrowski, R. Długosz, Comparison of various SC FIR filter structures on the basis of their CMOS realization and simulation in the PSPICE program, *Bulletin PAN*, Vol. 49, No. 1, 2001, pp. 59–79.

[35] A. Dąbrowski, D. Cetnarowicz, R. Długosz, P. Pawłowski, Design and optimisation of integrated CMOS FIR SC Channel filter for a GSM Receiver, *Proceeding of European Conference on Circuit Theory and Design*, pp. I.265–I.268, Helsinki, 28-31 August 2001

[36] R. Długosz, A. Dąbrowski, Comparison of Chip Area For Different FIR Filter Structures in CMOS Technology, *Proceeding of the 4th International Conference of Mixed Design of Integrated Circuits and Systems*, Poznanń 1997, pp. 341–346

[37] R Długosz, A. Dąbrowski, CMOS Realization and Comparison of Basic SC FIR Filter Structures, *Proceeding of the 5th International Conference of Mixed Design of Integrated Circuits and Systems*, Łódź 1998, pp. 281–286

[38] R. Długosz, A. Dąbrowski, Design of the multiphase clocks systems for SC FIR filter structures, *Proceeding of the 6th International Conference of Mixed Design of Integrated Circuits and Systems*, Kraków 1999, pp. 373–378

[39] R. Długosz, A. Dąbrowski, P. Kardyś, Design of FIR SC Filter for GSM Receiver, *Proceeding of the 7th International Conference of Mixed Design of Integrated Circuits and Systems*, Gdynia 2000, pp. 413–418

[40] D. Cetnarowicz, A. Dąbrowski, Design principles for FIR SC GSM channel filers, *Proceeding of the 7th International Conference of Mixed Design of Integrated Circuits and Systems*, Gdynia 2000, pp. 419–424

[41] R. Długosz, A. Dąbrowski, P. Pawłowski, Design of the SC FIR channel filter for GSM receiver in CMOS technology, *Proceeding of the 8th International Conference of Mixed Design of Integrated Circuits and Systems*, Zakopane 2001, pp. 487–492

[42] R. Długosz, A. Dąbrowski, P. Pawłowski, Design and measurement results of the GSM SC FIR channel filter realized in CMOS 0.8 μm technology, *Proceeding of the 9th International Conference of Mixed Design of Integrated Circuits and Systems*, Wrocław 2002, pp. 607–612

[43] A. Dąbrowski, R. Długosz, T. Marciniak, Realization of the clock control system for an FIR-SC filter using a digital signal processor, *Proceeding of the 10th International Conference of Mixed Design of Integrated Circuits and Systems*, Łódź 2003, pp. 629–632

[44] R. Długosz, A. Dąbrowski, Comparison of different SC FIR filter structures on the base of simulation in the PSPICE program, *Proceedings of the XXI National Conference on Circuit Theory and Electronic Networks*, Poznań-Kiekrz 1998, pp. 369–374

[45] D. Cetnarowicz, A. Dąbrowski, R. Długosz, P. Kardyś, Design of the Switched-Capacitor Channel Filter Structures for GSM, *Proceedings of the XXII National Conference on Circuit Theory and Electronic Networks*, Stare Jabłonki 1999, pp. 125–134

[46] A. Dąbrowski, R. Długosz, A conception for SC FIR Filter Structures Based on Higher Order Even-Odd Delay Elements, *Proceedings of the International Conference on Circuits and Electronic Systems*, Świeradów Zdrój 2002, pp. 287–292

[47] A. Dąbrowski, R. Długosz, P. Pawłowski, M. Moszczyński, Design of the FIR GSM Channel Filter structures in CMOS 0.8 μm technology, *Proceedings of the International Conference on Circuits and Electronic Systems*, Świeradów Zdrój 2002, pp. 209–214

[48] R. Długosz, A. Dąbrowski, Design and optimization of decimation filters for sigma-delta modulators, *Proceedings of the Signal Processing Workshop*, Poznań 2000, pp. 19–24

[49] R. Długosz, A. Dąbrowski, P. Pawłowski, Design of hardware multiphase clock systems for SC FIR filters, *Proceedings of the Signal Processing Workshop*, Poznań 2002, pp. 69–73

[50] D. Cetnarowicz, A. Dąbrowski, R. Długosz, T. Marciniak, Analog Versus Digital FIR Filters, *Proceedings of the Signal Processing Workshop*, Poznań 2002, pp. 63–68

[51] R. DługoszA. Dąbrowski, P. Pawłowski, Design, optimization and comparison of SC FIR filters, *Proceedings of the Signal Processing Workshop*, Poznań 2003, pp. 53–58

[52] A. Dąbrowski, R. Długosz, T. Pawłowski, Koncepcja programu komputerowego do syntezy analogowych filtrów dyskretnych FIR SC, *Materiały Konferencji Zastosowania Komputerów w Elektrotechnice*, Poznań - Kiekrz 2002, pp. 59–62 (in Polish)

[53] A. Dąbrowski, D. Cetnarowicz, T. Marciniak, R. Długosz, Implementacja algorytmów cyfrowego przetwarzania sygnałów z wykorzystaniem Code Composer Studio i procesorów sygnałowych rodziny TMS, *Materiały Konferencji Zastosowania Komputerów w Elektrotechnice*, Poznań - Kiekrz 2002, pp. 123–126 (in Polish)

[54] A. Dąbrowski, D. Cetnarowicz, T. Marciniak, R. Długosz, Separacja sygnałów metodą analizy niezależnych składowych, *Materiały Konferencji Zastosowania Komputerów w Elektrotechnice*, Poznań - Kiekrz 2002, pp. 115–118 (in Polish)

[55] *Cadence design tools Tutorial – http://vlsi.wpi.edu/cds*

[56] Atmel Corporation, *8-bit AVR Microcontroller with 1K Byte In-System Programmable Flash AT90S1200, Rev 0838F-10/2000*, Atmel Corporation 2001

[57] Atmel Corporation, *AVR Instruction Set*, Atmel Corporation 2001

[58] Altera, *Digital Library*, July 2002 CD-ROM Edition

[59] Altera *MAX+PLUS II 10.1 Student Edition Programmable Logic Development Software*, CD-ROM Edition

[60] Intersil, *1.4MHz, Low Power CMOS Operational Amplifiers ICL7611, ICL7612*, Intersil Corporation 1999

[61] Analog Devices, *Ultralow Power, Rail-to-Rail Output Operational Amplifiers OP181/OP281/OP481*, Analog Devices, Inc., 1996

[62] Analog Devices, *CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifiers with Shutdown AD8591/AD852/AD8594*, Analog Devices, Inc., 1999

[63] STMicroelectronics, *HCF4013B Dual D type flip-flop*, STMicroelectronics 2001

[64] F.A. Cherigui, *Cadence Full Custom IC Design Guidelines*, Cole Polytechnique Ederale de Lausanne 1999

List of author's publications

1. A. Dąbrowski, R. Długosz, Chip area estimation for SC FIR filter structures in CMOS technology, in *Mixed Design of Integrated Circuits and Systems*, Kluwer, Boston 1998, pp. 143–148.

2. A. Dąbrowski, R. Długosz, Comparison of various SC FIR filter structures on the basis of their CMOS realization and simulation in the PSPICE program, *Bulletin PAN*, Vol. 49, No. 1, 2001, pp. 59–79.

3. A. Dąbrowski, D. Cetnarowicz, R. Długosz, P. Pawłowski, Design and optimisation of integrated CMOS FIR SC Channel filter for a GSM Receiver, *Proceeding of European Conference on Circuit Theory and Design*, pp. I.265–I.268, Helsinki, 28-31 August 2001

4. R. Długosz, A. Dąbrowski, Comparison of Chip Area For Different FIR Filter Structures in CMOS Technology, *Proceeding of the 4th International Conference of Mixed Design of Integrated Circuits and Systems*, Poznanń 1997, pp. 341–346

5. R Długosz, A. Dąbrowski, CMOS Realization and Comparison of Basic SC FIR Filter Structures, *Proceeding of the 5th International Conference of Mixed Design of Integrated Circuits and Systems*, Łódź 1998, pp. 281–286

6. R. Długosz, A. Dąbrowski, Design of the multiphase clocks systems for SC FIR filter structures, *Proceeding of the 6th International Conference of Mixed Design of Integrated Circuits and Systems*, Kraków 1999, pp. 373–378

7. R. Długosz, A. Dąbrowski, P. Kardyś, Design of FIR SC Filter for GSM Receiver, *Proceeding of the 7th International Conference of Mixed Design of Integrated Circuits and Systems*, Gdynia 2000, pp. 413–418

8. R. Długosz, A. Dąbrowski, P. Pawłowski, Design of the SC FIR channel filter for GSM receiver in CMOS technology, *Proceeding of the 8th International Conference of Mixed Design of Integrated Circuits and Systems*, Zakopane 2001, pp. 487–492

9. R. Długosz, A. Dąbrowski, P. Pawłowski, Design and measurement results of the GSM SC FIR channel filter realized in CMOS 0.8 μm technology, *Proceeding of the 9th International Conference of Mixed Design of Integrated Circuits and Systems*, Wrocław 2002, pp. 607–612

10. A. Dąbrowski, R. Długosz, T. Marciniak, Realization of the clock control system for an FIR-SC filter using a digital signal processor, *Proceeding of the 10th International Conference of Mixed Design of Integrated Circuits and Systems*, Łódź 2003, pp. 629–632

11. R. Długosz, A. Dąbrowski, Comparison of different SC FIR filter structures on the base of simulation in the PSPICE program, *Proceedings of the XXI National Conference on Circuit Theory and Electronic Networks*, Poznań-Kiekrz 1998, pp. 369–374

12. D. Cetnarowicz, A. Dąbrowski, R. Długosz, P. Kardyś, Design of the Switched-Capacitor Channel Filter Structures for GSM, *Proceedings of the XXII National Conference on Circuit Theory and Electronic Networks*, Stare Jabłonki 1999, pp. 125–134

13. A. Dąbrowski, R. Długosz, A conception for SC FIR Filter Structures Based on Higher Order Even-Odd Delay Elements, *Proceedings of the International Conference on Circuits and Electronic Systems*, Świeradów Zdrój 2002, pp. 287–292

14. A. Dąbrowski, R. Długosz, P. Pawłowski, M. Moszczyński, Design of the FIR GSM Channel Filter structures in CMOS 0.8 μm technology, *Proceedings of the International Conference on Circuits and Electronic Systems*, Świeradów Zdrój 2002, pp. 209–214

15. R. Długosz, A. Dąbrowski, Design and optimization of decimation filters for sigma-delta modulators, *Proceedings of the Signal Processing Workshop*, Poznań 2000, pp. 19–24

16. R. Długosz, A. Dąbrowski, P. Pawłowski, Design of hardware multiphase clock systems for SC FIR filters, *Proceedings of the Signal Processing Workshop*, Poznań 2002, pp. 69–73

17. D. Cetnarowicz, A. Dąbrowski, R. Długosz,T. Marciniak, Analog Versus Digital FIR Filters, *Proceedings of the Signal Processing Workshop*, Poznań 2002, pp. 63–68

18. R. DługoszA. Dąbrowski, P. Pawłowski, Design, optimization and comparison of SC FIR filters, *Proceedings of the Signal Processing Workshop*, Poznań 2003, pp. 53–58

19. A. Dąbrowski, R. Długosz, T. Pawłowski, Koncepcja programu komputerowego do syntezy analogowych filtrów dyskretnych FIR SC, *Materiały Konferencji Zastosowania Komputerów w Elektrotechnice*, Poznań - Kiekrz 2002, pp. 59–62 (in Polish)

20. A. Dąbrowski, D. Cetnarowicz, T. Marciniak, R. Długosz, Implementacja algorytmów cyfrowego przetwarzania sygnałów z wykorzystaniem Code Composer Studio i procesorów sygnałowych rodziny TMS, *Materiały Konferencji Zastosowania Komputerów w Elektrotechnice*, Poznań - Kiekrz 2002, pp. 123–126 (in Polish)

21. A. Dąbrowski, D. Cetnarowicz, T. Marciniak, R. Długosz, Separacja sygnałów metodą analizy niezależnych składowych, *Materiały Konferencji Zastosowania Komputerów w Elektrotechnice*, Poznań - Kiekrz 2002, pp. 115–118 (in Polish)

22. A. Dąbrowski, R. Długosz, T. Marciniak, Koncepcja internetowej wizualizacji i sterowania gniazdem produkcyjnym, *Materiały Poznańskich Warsztatów Telekomunikacyjnych*, pp. 3.3.1–3.3.6, Poznań 1999 (in Polish)

23. D. Cetnarowicz, A. Dąbrowski, R. Długosz, P. Kardyś, T. Marciniak, Wizualizacja Procesów Elastycznego Wytwarzania, *Materiały Poznańskich Warsztatów Telekomunikacyjnych*, pp. 3.2.1–3.2.6, Poznań 2000 (in Polish)