Novel CMOS Analog Pulse Shaping Filter for Solid-State X-Ray Sensors in Medical Imaging Systems

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Abstract. A new idea as well as CMOS implementation of a pulse-shaping filter useful in nuclear medicine to realize a multi-element detection by means of a multi-channel readout front-end ASIC have been presented. The filter changes the shape of pulses delivered by a charge amplifier in order to increase the detection speed and robustness. By canceling falling edges of the pulses, a significant increase in the pulse counting rate has been reached (between 3 and 10 MSps in a single channel). The filter takes advantage of a RESET function that is controlled by an asynchronous multiplexer. Including only two resistors, two capacitors and four configuration transistors, it is simpler than other solutions reported to overcome this problem. The proposed shaper together with a peak detector, that receives the shaper signals, dissipates a small amount of power (about 80 μW) for 1V supply voltage. When being inactive, i.e. waiting for the next pulse, the circuit consumes only 200 nW of power.

Keywords: Medical imaging, pulse shaping filter, nuclear medicine.

1 Introduction

Specialized integrated circuits (ASIC) are important part of modern apparatus used in medical imaging. Nuclear medicine techniques use pharmaceuticals that have been labeled with radionuclides and introduced to the patient's body. The role of imaging devices is to detect the emitted X or gamma rays and convert it to an eletrical voltage signal. In most of existing imaging devices, data conversion consists of several steps. First, the X or gamma photons are converted into the visible light using the scintillator and then the light is transformed, using photomultiplier, to a burst of electrons. Multi-step data conversion in such systems is a source of errors, which in practice limit the image resolution.

* Fellow of the EU Marie Curie International Outgoing Fellowship.

E. Kącki, M. Rudnicki, J. Stempczyńska (Eds.): Computers in Medical Activity, AISC 65, pp. 155–165.
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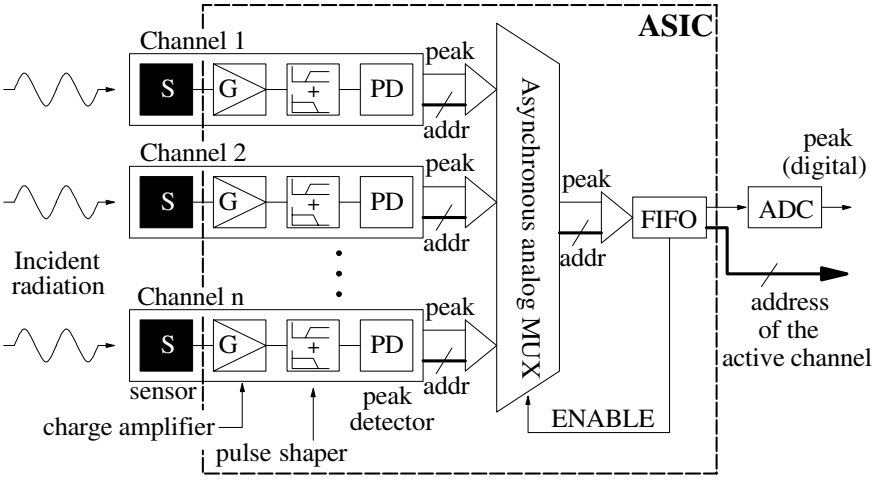

Fig. 1. General block diagram of a typical multi-channel front-end ASIC for multi-element detection systems [3]

In solid-state detectors that recently have been introduced to the market, the X or gamma photons absorbed by an array of sensors are directly converted into an equivalent charge pulses, which may be then processed using the readout multi-channel detecting system [1]. Such diagnostic tools allow for creating medical images of the human body for different clinical purposes.

Front-end readout ASICs, being core circuits in such systems, are subject of research efforts since many years [2, 3]. The observed development in this area is possible due to a continuous progress in microelectronics but also due to development of new circuit solutions, which minimize both chip area and power dissipation, thus allowing for increasing a number of channels integrated in a single chip. In current systems of this type, the number of channels varies between several dozen to several hundreds. Each channel usually contains a charge amplifier (CHA), a pulse shaper (PS) and a peak detector (PD) as show in Fig. 1 [2]. The signal processing scheme in each channel relies on detection of an incident radiation by an associated sensor, which generates an equivalent amount of charge. This charge usually is very small [4] (several dozen aC for 1 keV X-rays) and exhibits random distribution over time for particular events. The task of the CHA circuit is to amplify this charge and store it in a capacitor, generating a voltage proportional to the charge amount for a given radiation event. When this process is quick enough, the PS block gets the signal that can be modeled as a Haeviside step function. The shaper is in practice a band-pass filter, which converts the input step function into a pulse of a given peaking time and amplitude which is proportional to the step value. The role of the PD block (next circuit in the chain) is to store the amplitude in a memory element and set up the flag signal.

2 Proposed Pulse Shaping Band-Pass Filter

For particular radiation events, the CHA circuit generates signals that can be modeled as a Haeviside step function, which in the subsequent PS circuit is converted into a corresponding appropriately shaped impulse, whose amplitude is proportional to the value of this step.

There are several problems encountered in the shaping operation [4]. In real electronic systems, the useful signal is accompanied by a noise, which in this case alters the peak amplitude, introducing a random error to each impulse. To limit the noise spectrum, the useful signal bandwidth at the PS output should be as narrow as possible. Unfortunately, in this case the impulse peak is wide. Although wide peaks simplify the structure of the PD circuit, giving more time for detection and data storage, it decreases the maximal count rate of the channel.

An example implementation of the PS block that overcomes this problem has been described in [4]. In [4], to form wide peaks with short falling edges, the PS block has been realized as a serial connection of passive CR and RC filters, with amplifiers inserted between particular filters to correct the signal amplitude. In this solution, the first block is a band-pass filter shown in Figure 2, while in the next stages additional low-pass RC filters are used.

The first part of our CR-RC circuit is a high-pass filter (R_1C_1), often referred to as a differentiator [4]. To be more precise, this is a differentiator with some inertia mechanism. A "pure" differentiator could not be used in this application as its output amplitude does not depend on the input amplitude, but only on raising time (slope) of the input step function. The problem is that it is not possible to ensure equal rising times at the CHA output because charge impulses received from the sensor have random distributions over time. They can be, for instance, wide and fuzzy or high and narrow. Using a differentiator with an inertia makes the problem insignificant provided that the filter decay time constant is sufficiently large compared to raising time of the input step signals.

The second subcircuit shown in Figure 2 is a low-pass filter (R_2C_2), which is often referred to as an integrator [4]. In fact, this is an inertia circuit whose behavior at higher frequencies is similar to the integrator. For an input signal defined as a step function, the entire CR-RC block operates as a second order inertia circuit excited by a Dirac's delta function. In this case, peaking time of the resultant impulse is constant for a wide amplitude range of the input step function.

Notice that the shaping operation is only possible in the presence of inertia in both the C_1R_1 and R_2C_2 filters. Time constant of the C_1R_1 high-pass filter sets up the width of the impulse. This parameter must be matched to the worst case scenario, i.e. when

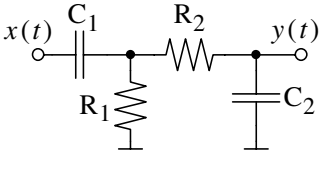

Fig. 2. Simplified electrical scheme of the CR-RC band-pass pulse shaping filter [4]. The amplifiers used to the amplitude correction are not presented in the figure.

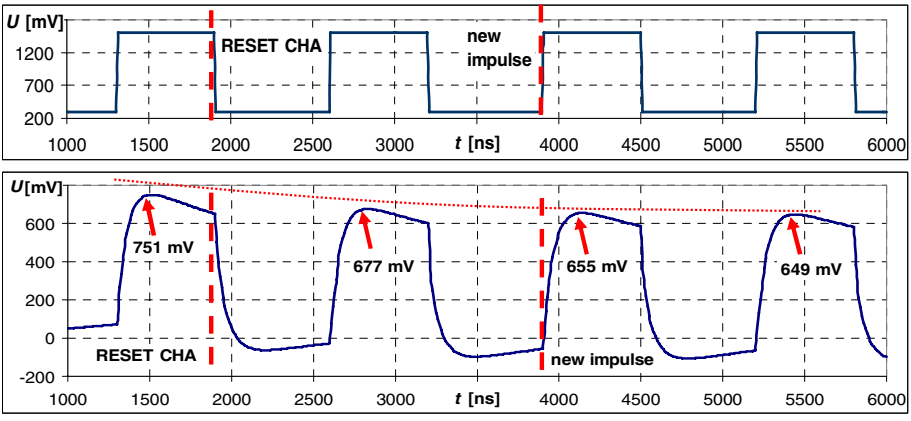

Fig. 3. Input (upper) and output (lower) signals of the pulse shaping filter shown in Fig. 2 in case when input events occur too frequently and pulses overlap each other

the raising time of the input step function is the longest. Increasing this parameter makes shaper's output insensitive to the raising time of the input step function, but this limits the count rate of the channel. The time constant of the R_2C_2 low-pass filter influences both raising time and amplitude of the output signal.

The other important problem related to the pulse shaping is overlapping of adjacent pulses, resulting from long falling edges. Theoretically, the falling edges never vanish, but in practice, when a sufficiently long time is allocated then impulses can be assumed to be independent events. When this time is to short, a new event triggers the transition state with non-zero initial conditions, which introduce additional errors to the output signal. The additional problem is that resetting the CHA circuit means a negative step function at the PS input. This starts a new transition state with non-zero initial conditions, which is illustrated in Figure 3. Note that adjacent impulses occur too frequently causing random errors of the impulse amplitudes.

Key parameter of the detection system is peaking time. Therefore, the impulse falling edge can be considered as a parasitic effect that must be optimized to increase capacity of the channel. Using many CR and RC filters in the shaper described in [4] allows for increasing the decay time constant, but this solution is not optimal due to several reasons. When the number of low-pass filters in the chain increases, a performance improvement resulting from additional stages is smaller and smaller with an increase of stages. For example, adding only one low-pass filter to an existing one brings a better improvement than adding additional four filters to existing four [4]. The problem is that each additional RC filter enlarges both the chip area and power consumption (due to additional amplifiers).

To eliminate this drawback, we propose a new solution, shown in Figure 4, where only a single CR-RC filter is used. In this circuit, a naturally long decay time has been shortened using a RESET signal. The applied mechanism quickly discharges both capacitors (C_1 and C_2) and the channel is ready for a new shaping operation with zero initial conditions. This is illustrated in Figure 5. The shaper is excited by the same input signal like in the experiment shown in Figure 3.

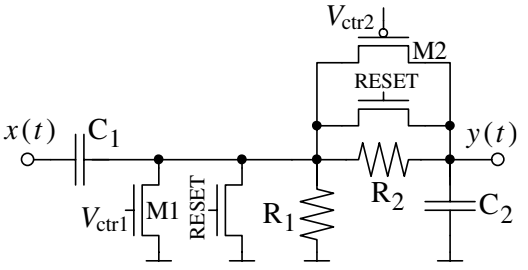

Fig. 4. The proposed pulse shaping filter with built-in RESET and programming functions

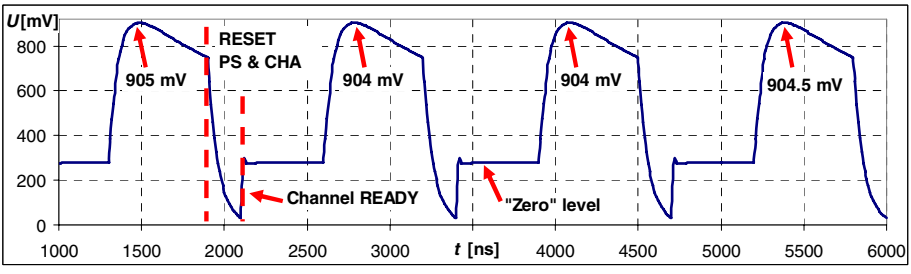

Fig. 5. Output signal of the proposed pulse shaping filter shown in Figure 4

The proposed solution possesses several important advantages. First, the circuit chip area is relatively small (equal to 0.005 mm^2) because of the shaper simplicity (only four passive elements, i.e. C_1=1.7pF, C_2=0.8pF, R_1=500k, R_2=100k). This is important in detecting systems with many channels, where each channel must include the shaper. Another advantage is a very low power consumption of the filter as no correction amplifiers are needed.

2.1 The Shaper Adjusting Capabilities

One of our objectives was to realize a shaping filter that enables controlling both the peaking time and amplitude of the obtained impulse. *S*-domain block diagram of the shaper of Figure 4 is shown in Figure. 6. Its input signal, $X(s)$, is assumed to be a Haeviside step-function voltage, while $Y(s)$ is output voltage of the filter.

Neglecting in Figure 4 the presence of the transistors, the shaper output signal is described by:

$$Y(s) = H(s)X(s) = A\frac{R_1C_1}{s^2R_1R_2C_1C_2 + s\left(R_1C_1 + R_2C_2 + R_1C_2\right) + 1} \tag{1}$$

Assuming that R_1 and R_2 as well as C_1 and C_2 are linearly related, i.e:

$$R_2 = aR_1 \quad \text{and} \quad C_2 = bC_1, \tag{2}$$

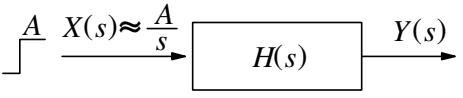

Fig. 6. Block diagram of the pulse shaper in *s*-domain

where: a and b are constant coefficients. Poles of (1), s_1 and s_2, can be expressed as:

$$s_1 = \frac{-(1+ab+b)-\sqrt{1+a^2b^2+b^2+2b+2ab^2-2ab}}{2abR_1C_1} = \frac{k_1}{R_1C_1} \tag{3}$$

$$s_2 = \frac{-(1+ab+b)+\sqrt{1+a^2b^2+b^2+2b+2ab^2-2ab}}{2abR_1C_1} = \frac{k_2}{R_1C_1} \tag{4}$$

Finally, the shaper output signal described in s and time domains takes to forms:

$$Y(s) = A\frac{1}{abR_1C_1(s_2-s_1)}\left(\frac{1}{s-s_2}-\frac{1}{s-s_1}\right) \tag{5}$$

$$y(t) = \frac{1}{\sqrt{1+a^2b^2+b^2+2b+2ab^2-2ab}}\left(e^{s_2t}-e^{s_1t}\right) \tag{6}$$

From (6) it is seen that amplitude of the output signal (peak value) remains unchanged as long as relations between the R_1 and R_2 are kept constant as well as that between C_1 and C_2, i.e. when the dimensionless parameters, a, b, k_1, k_2, in (3), (4) and (6) remain unchanged. As a consequence, by proper varying values of R_1, C_1, R_2, C_2, we can influence only the pole values (s_1 and s_2) and control only peaking time, causing no variations in amplitude of the output signal, which is shown in Figure 7 (MATLAB simulation results). As can be seen from Figure 7, for $R_1/R_2 = 10$ the amplitude is approximately equal to 0.6V and for $R_1/R_2 = 2.5$ equal to about 0.5V.

To make the circuit to be useful in practice, two transistors marked in Figure 4 as M1 and M2 have been added to our filter. These transistors are controlled by means of two biasing voltages V_{ctr1} and V_{ctr2}. Being connected in parallel with R_1 and R_2, respectively, they enable reducing the $R1$ and $R2$ values and varying in this way the R_1C_1 and R_2C_2 time constants of the filter and its output impulse shape. This allows us to perform wider laboratory tests of the system. Example impulses obtained for the same input step function but different values of the bias voltages V_{ctr1} and V_{ctr2} are illustrated in Figure 8. The five curves plotted in Figure 8 correspond to the points A, B, C, D, F in Figure 9, where the horizontal axis represents the V_{ctr1} and the vertical one the V_{ctr2} biasing voltages. In this example, the longest peaking time (Δt =190 ns) is approximately 3 times bigger than the shortest one (Δt = 60 ns).

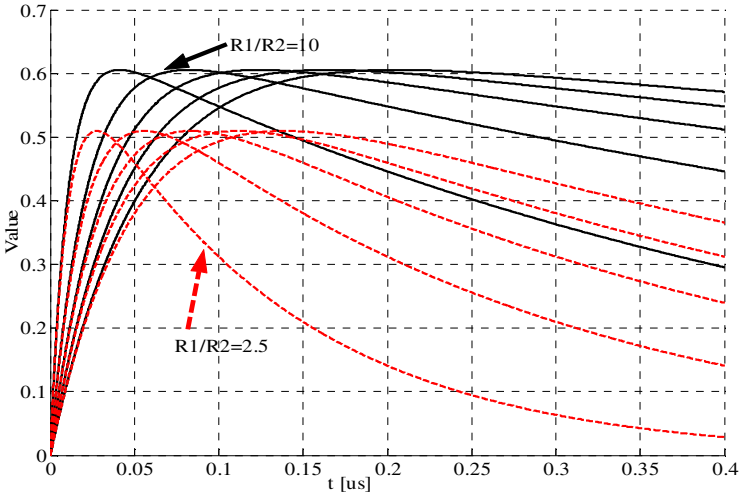

Fig. 7. Theoretical curves of the pulse shaping filter for selected values of passive elements and constant *a* and *b* coefficients

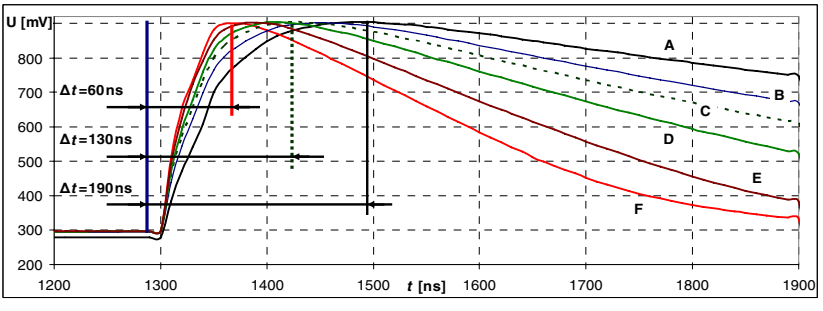

Fig. 8. Output signal of PS for different values of the biasing V_{ctr1} and V_{ctr2} voltages

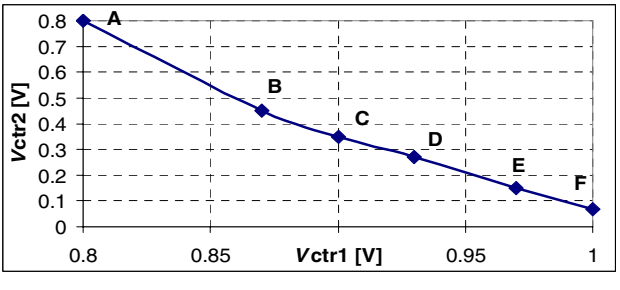

Fig. 9. Values of the V_{ctr1} and V_{ctr2} biasing voltages used in HSPICE simulations of Figure 8

3 Peak Detector

Peak detector takes impulses from the shaping filter. The detector precision is essential and has a direct influence on the output-image pixel-depth. In our studies, a peak detector circuit proposed in [5] has been used. The circuit is shown in Figure 10 together with a flag (FL) generation circuitry. Its operation is based on two delay elements controlled by a two-phase clock. The circuit features a simple structure, resulting in a low chip area and low power dissipation. Moreover, a relatively high precision (as high as 99 %) can be achieved.

This circuit works as follows. The V_{in}(t) input voltage signal enters the C_{st} capacitor as well as the MN1 transistor that operates in a diode configuration, limiting the input signal amplitude of the transistors MN2 and MN3. This signal is next sampled and held and converted to currents that flow through MN2 and MN3. Both capacitors at the MN2 and MN3 gates have values of 20 fF. The appropriate configuration of switches causes the recent samples to be always copied to the current mirror MP1-MP2 and then to the comparator as a positive value. Samples stored previously are transferred to the current mirror MP3-MP4 and then to the comparator as a negative value, using the current mirror MN4-MN5. As a result, when the input signal is rising,

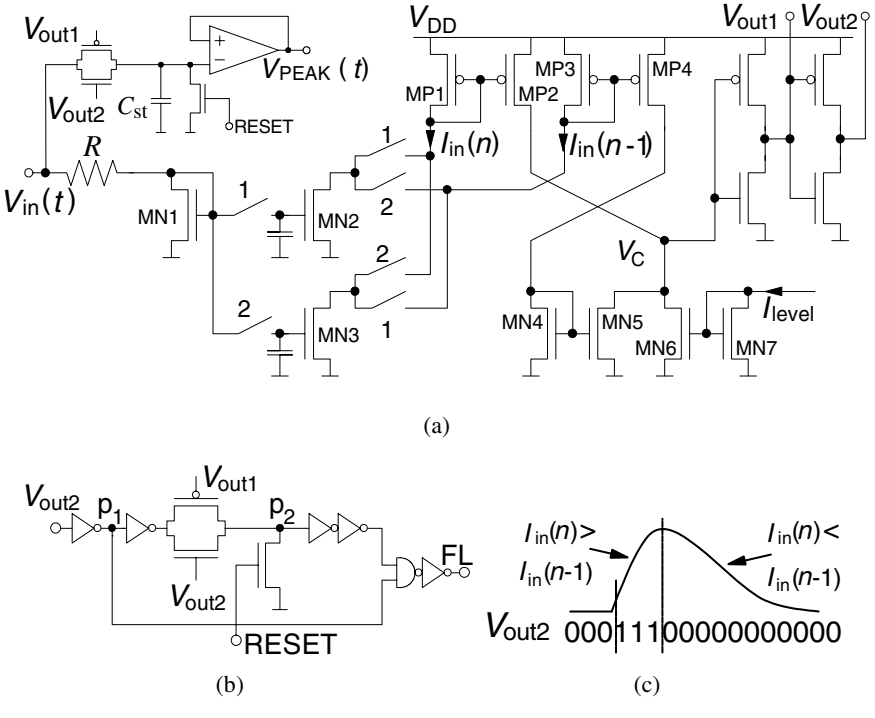

Fig. 10. Peak detector reported in [5]: (a) latching circuit with a switched current circular delay line and a voltage-mode sample-and-hold element, (b) flag generation circuitry, (c) the latch circuit principle of operation

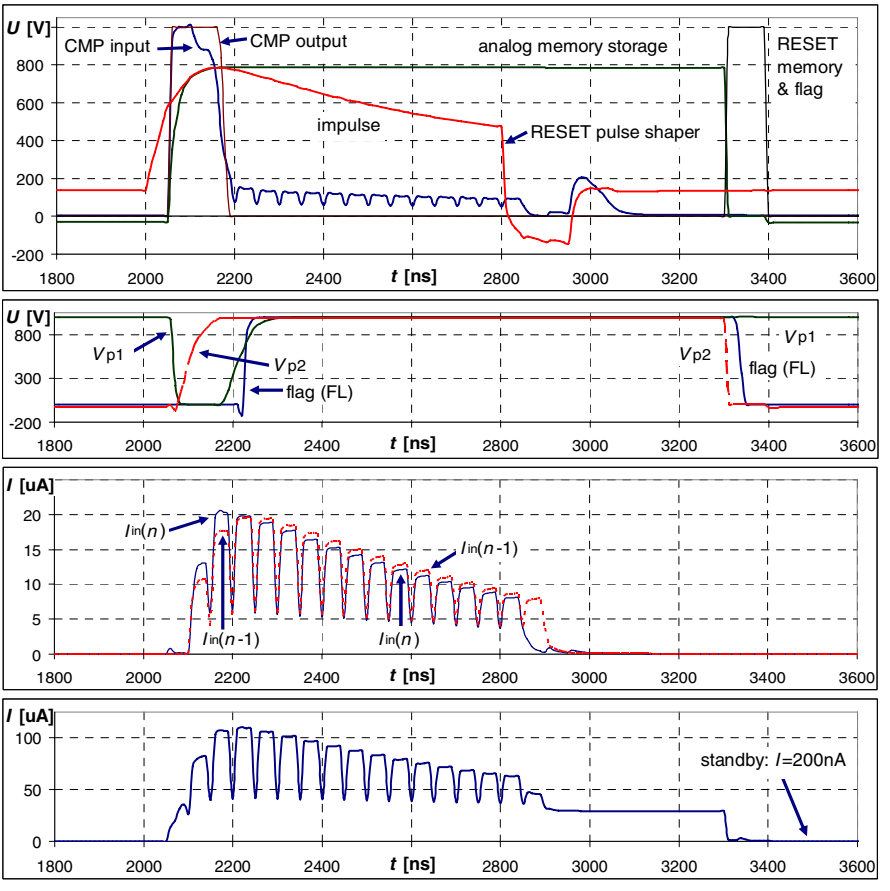

Fig. 11. Postlayout simulation results of the pulse shaping block together with the peak detector

$I_{in}(n)$ is larger than $I_{in}(n\text{-}1)$ and the comparator output enables tracking the input signal of the S&H element shown in the upper left corner of Figure 10 (a). When both signals became equal, i.e. when a peak is reached, the S&H element latches the peak value across the capacitor C_{st} and sets the FL signal to logical "1" by means of the circuit shown in Fig. 10 (b). The detector operation principle is illustrated in Figure 10 (c). Experimental results presented in [5] concern a PD block operating as a separate block, with the input sinus signal applied. In this paper, we present simulation results of an entire channel, where both the proposed PS and PD blocks are joined together.

Postlayout simulation results are shown in Figure 11. Operation of the main (latching) block is presented in the upper panel. The waveforms of the flag generation circuit are shown in the second panel. Note that the FL signal is set up only when the impulse is already stored and the comparator output becomes logical "0" [5]. This allows for reading out this data by an MUX circuit just after the signal fully settles in the PD analog memory.

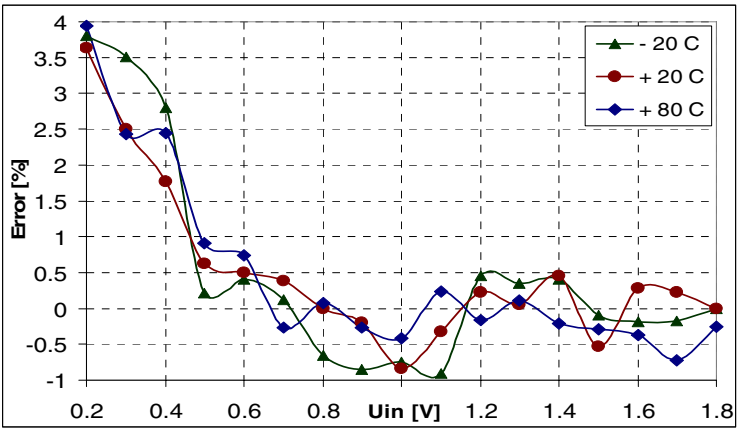

Fig. 12. Accuracy of a single channel (PS and PD blocks), expressed by amplitude error versus the input step voltage in a wide temperature range for standard 1.8 V supply voltage

The third panel illustrates operation of the delay line. When the input signal is rising then $I_{in}(n)$ is greater than $I_{in}(n\text{-}1)$. When the input signal reaches the peak, the $I_{in}(n)$ current becomes smaller, which switches over the comparator output.

A total current consumption in both the PS and PD blocks is shown in the bottom panel, for the supply voltage equal to 1.1 V. After reading out the data, both circuits are reset and channel goes to a power-down mode, where power dissipation becomes small and is below 0.5 μW. This is a very important feature, as both the PS and PD blocks are used in a large number of the system channels.

Accuracy of the PS-PD pair, illustrated in Figure 12, was tested in a wide temperature range, using transistor models related to a standard TSMC CMOS 0.18 μm process. The obtained amplitude error is kept below 1 % in a wide range of amplitudes. For small amplitudes this error raises up reaching the value of about 4 % for $A = 0.2$V. This is not a serious problem, as the error is of systematic nature and can be easily corrected after the analog to digital output data conversion. After the error compensation, the resultant system accuracy at the level of 99.5 % is achievable.

4 Conclusions

This paper presents a new analog-digital CMOS circuit suitable to play a role of pulse shaping band-pass filter in medical imaging systems that take advantage of multi-element detection. Multi-channel readout ASIC's, where our circuit is to be included, are used as front-end blocks in such systems. Development of modern analog-digital ASIC's is associated, among others, with miniaturization of particular building blocks and optimization of their electrical schemes, which allows for enlarging the number of channels implemented on a single chip.

Our filter exhibits important advantages compared to other techniques applied for the pulse shaping purposes. Including only two resistors, two capacitors and four MOS transistors it occupies only 0.005 mm^2 of chip for a standard TSMC 0.18 μm

CMOS process. It is also effective in solving the problem of overlapping two adjacent impulses. The pulse overlapping problem degrades detection precision and speed considerably. Previous attempts to solve this problem were not fully satisfactory as regards power and area consumption. In our filter, the overlapping effect has been defeated without power and area enlargement, by applying a proper filter concept with a simple reset technique and proper designing its element values. This has lead to narrowing the impulses provided to the peak detector. As a result, the obtained impulses have the required width and peaking time can be retuned by means of two biasing voltages in the range from 60ns to 200 ns. The applied RESET function allows for canceling the impulse falling edge just after the data has been read out and the channel is immediately ready to process a new impulse. Not taking into account the input charge amplifier, a single channel in the readout ASIC dissipates during the data acquisition an average power of 80 μW from 1 V supply voltage. When awaiting a new impulse, the PS and PD blocks are in the power-down mode, dissipating only 200 nW. The circuit works properly in a wide range of supplies from 0.8 to 1.8 V.

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