Low Chip Area, Low Power Dissipation, Programmable, Current Mode, 10-bits, SAR ADC Implemented in the CMOS 130nm Technology

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***Abstract*—In this paper we present a novel successive approximation register (SAR) analog-to-digital converter (ADC) designed for the applications that demand many such converters working in parallel in a single chip. For this reason we have put a special emphasis on a very low chip area and low power dissipation. The ADC operates in the current-mode. The digital-to-analog converter (DAC), which is one of the components of the SAR ADCs, is in this case based on a concept of a two-stage split architecture that allows to obtain higher resolutions without a substantial increase of the chip area. As a result, the circuit implemented in the IHP CMOS 130nm technology occupies the area of only 0.01 mm^2. At data rate of 0.55 MSamples/s and 10-bits of resolution it dissipates an average power of 13.2 μW. The supply voltage equals 1.2 V. The proposed circuit is programmable. The 2-stage DAC is composed of 10 branches. If smaller resolutions are sufficient, we can select the branches which are used to perform the conversion. This allows to control, to some extent, data rate of the ADC and the power dissipation.**

***Index Terms*—SAR ADC, current mode, CMOS technology, low chip area, low power dissipation**

I. Introduction

Analog-to-digital converters (ADCs) can be classified as Nyquist rate and oversampled – based on sigmadelta modulators. The ADCs from the second group are preferred for very high bit resolutions. However, they demand very fast oversampling clock generator that makes them relatively low-speed architectures. Additionally, this controlling signal has to be very clean, as the clock jitter has a strong impact on the obtained signal-to-noise ratio (SNR) and thus the real resolution of the ADC. The Nyquist rate converters, on the other hand, are typically used in applications that require lower data resolutions and much higher data rates [1]. These converters usually belong to one of four main groups [1], [2]: flash, pipeline, foldinginterpolating and algorithmic. The last group comprises successive approximation register (SAR) converters, which are in our scope of interest in this paper.

Considering such parameters as data rate, output data resolution, and power dissipation, particular architectures are preferred in different types of applications. In flash ADCs, all bits are calculated in parallel, which makes them potentially the fastest of all approaches. The state-of-the-art converters of this type realized in a standard CMOS process operate with data rates of up to several gigahertz (GHz) [3], [4]. In this architecture, offset compensation is very important, since different offsets of particular comparators operating in a thermometer type conversion have a direct influence on the differential nonlinearity (DNL) of the inputoutput characteristics. The price for a high resolution and a high conversion rate is very high power dissipation, as the number of comparators (equal to $2^n - 1$, where n is the number of bits) is doubled with each additional bit. For this reason, flash converters are used in applications that demand high data rates, that accept low resolutions, typically in the range of 3 to 5 bits, and in which the power dissipation is of a secondary importance.

In contrast to flash converters, SAR ADCs with only one comparator allow to achieve very low power dissipations, but they are also relatively slow architectures, as only one bit is calculated per one clock cycle. To achieve higher conversion rates, several SAR blocks can be time interleaved. The interleaved architectures are more and more frequently explored in recent years [1], [5], [6], as Figure-of-Merit defined as data rate over the dissipated power is in this case much smaller than in the flash converters. For an example resolution of 8 bits, the flash ADC will contain 127 comparators, while the SAR interleaved converter only 8.

The SAR and the flash ADCs can be seen as basic architectures that offer relatively simple structures. These converters are often used as components in the pipelined and the folding-interpolating architectures that usually achieve larger resolutions (14 to 20 bits) [7]. For example, the conversion process in the pipelined ADC is composed of several steps as it is in the SAR ADC, but in contrary to the last one in each step the pipeline ADC calculates several bits in parallel, using low resolution flash ADCs.

While most SAR ADCs operate in the voltage-mode (charge-redistribution architecture), we propose an architecture based on the current-mode principle, as that mode enables to

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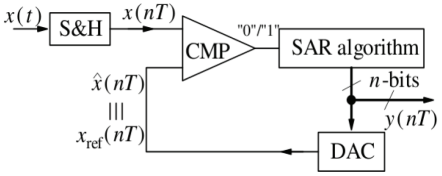

Fig. 1. A general idea of the SAR ADC.

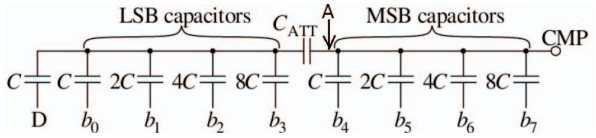

Fig. 2. Split-array technique used in voltage-mode SAR ADCs.

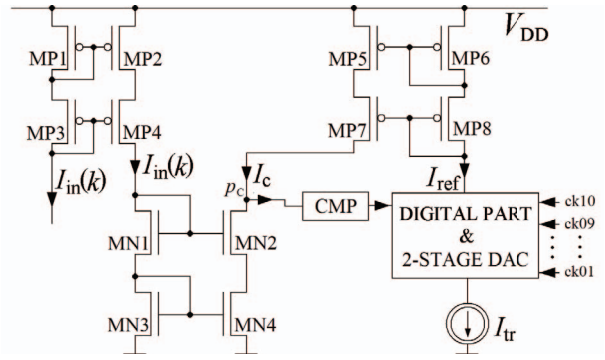

Fig. 3. General structure of the proposed current-mode SAR ADC.

design ADCs that occupy very small silicon area. Most V-mode SAR ADCs achieve the resolutions up to 8 bits. This results from the fact that the area of the DAC, realized in this approach as binary-weighted capacitor array, is doubled with each additional bit [8], [9]. As the capacitor array has to be recharged for each new sample, the bandwidth quickly decreases with increasing the resolution. To obtain higher resolutions various techniques are applied, briefly presented in next Section.

Current-mode converters can operate over a wide range of the input signals and thus data rates and power dissipation can be easily adjusted depending on requirements. In this paper we present a novel programmable 10-bit SAR ADC, implemented in the CMOS 130 nm technology that occupies the area of only 0.01 mm^2 and achieves data rates in-between 0.2 and 3 MSamples/s at power dissipation of 2.5–14 μW. The chip area is one of the most important features here, as the aim is to use such converters in the applications that require many such converters working in parallel.

Target applications of the proposed ADC include:

- Low power medical diagnostics systems based on Wireless Body Area Networks (WBAN),
- Low power analog artificial neural networks implemented in hardware,
- Analog Front End (AFE) ASIC used in nuclear medicine,

II. SAR ADC – An Overview

A typical classic SAR converter contains four main components, as shown in Figure 1, i.e., the sample-and-hold element (S&H) that is used to acquire the input signal, a comparator, a digital-to-analog converter (DAC) that provides the reference signal to the comparator, and the control-logic circuitry that controls the calculation algorithm. In SAR ADC, a binary search algorithm is used in the conversion of the analog signal into its digital representation. In this algorithm in following clock cycles particular bits are set to 1, starting from the most significant bit (MSB). The DAC supplies an equivalent reference signal that is compared by the comparator with the input signal stored in the S&H circuit. Depending on which signal is larger (input or reference), the comparator either resets or maintains particular bits until the least significant bit (LSB) is tested.

A. Optimization Techniques of the Voltage-Mode SAR ADCs

Various optimization techniques have been proposed in the literature. Since the silicon area and data rate of such converters strongly depend on total capacitance of the capacitor array, the optimization process usually relies on minimizing this capacitance. Minimization of the smallest capacitor – unit capacitor (UC) – is risky, as in this way we increase an influence of the parasitic capacitances that leads to a reduction in the precision of the ADC.

Another method that gained popularity in recent years takes advantage of the split-array technique [10]. In this case, instead of using the binary-weighted capacitor array, an additional attenuation capacitor, C_{att}, is used that divides the array into two subarrays that calculate LSBs and MSBs, respectively. Such split array is shown in Figure 2. The capacitance of the C_{att} capacitor should have a value that satisfies the following equation:

$$C_{\mathrm{att}} = C \cdot \frac{\sum \mathrm{LSBcapacitors}}{\sum \mathrm{MSBcapacitors}} \tag{1}$$

In this situation the resultant values of LSB capacitances that the comparator "sees" at point A are smaller by a factor of $2 \cdot i$, where i is the number of the LSB capacitors.

B. Proposed Current-Mode SAR ADC

The proposed ADC, shown in Fig. 3, is based on the current-mode technique in which the DAC block is realized as a multi-output current mirror, with particular output transistors being binary weighted. The conversion algorithm is similar to the one performed in the V-mode approach. Particular bits set up the components of the reference current, which is then compared with the input signal in the I-mode comparator. The I-mode approach offers several advantages. One of them is a very small energy consumed during the calculation of a single bit. In contrary to charge-redistribution architectures, the currents that flow in the current-mode DAC must charge only parasitic capacitances in particular transistors. As a result, such converters can potentially achieve better performance. Another

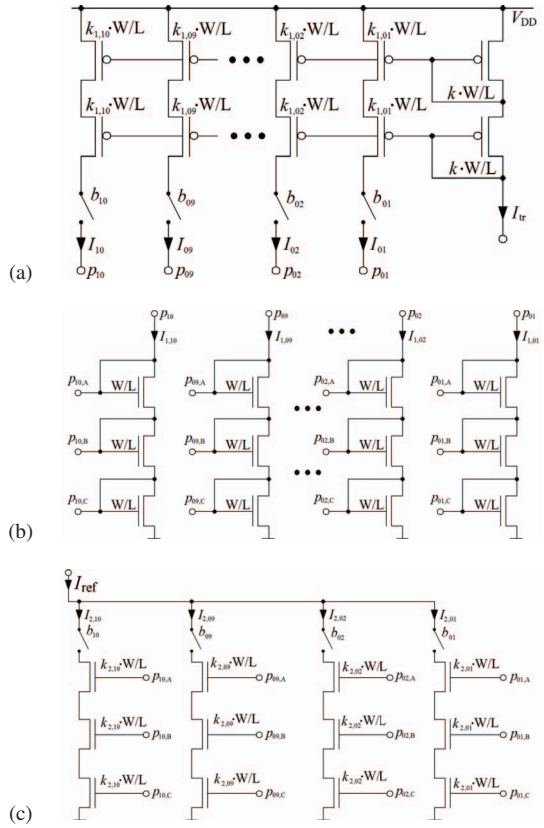

Fig. 4. Structure of the 2-stage current-mode DAC.

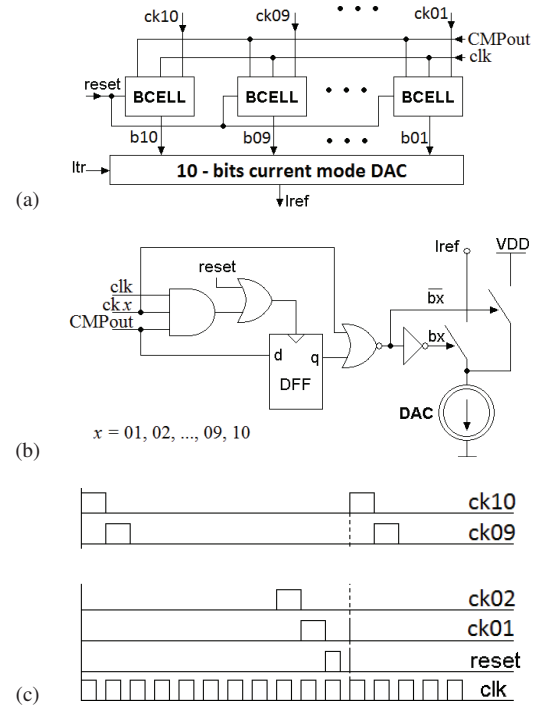

Fig. 5. Digital part of the proposed converter: (a) General structure, (b) single cells (BCELL) that control particular conversion steps, (c) 10-phases controlling clock generator.

advantage is a very small chip area, since the DAC block in this case does not contain large capacitors.

The disadvantage of the I-mode SAR ADCs is sensitivity of the DAC to transistor mismatch. To minimize this problem one can increase the sizes of the smallest transistor with unit width (UW), but this in practice limits the resolution of the converter, as the MSB transistors become very large.

To solve this problem we used another technique [1], in which the DAC is realized as a cascade connection of a multistage PMOS (1^{st} stage) current mirror and n NMOS CMs (2^{nd} stage), in which transistors are not binary weighted. Spreads between transistor in particular intermediate CMs are much smaller than in a single-stage binary-weighted approach. The structure of the I-mode 2-stage DAC is shown in Fig. 4. An input current I_{tr} that controls the upper range of the reference current I_{ref} is copied ten times in the cascode PMOS CM with the following gains:

$$k_{1,x} = \{1, 1, 2, 2, 4, 4, 8, 16, 16, 16\}/k \tag{2}$$

Resultant currents I_x flow to the next stage, composed of ten cascode NMOS CMs with the following gains:

$$k_{2,x} = \{1, 2, 2, 4, 4, 8, 8, 8, 16, 32\} \tag{3}$$

The resultant output currents $I_{2,x}$ are binary weighted as in the classical single-stage approach.

A proper selection of the coefficients $k_{1,x}$ and $k_{2,x}$ enables significant minimization of the spread between transistor sizes that allows for increasing the size of all transistors, thus improving matching. For the resolution of 10 bits the sum of transistor widths of all transistors in a single-stage approach would equal $(1023+k)\cdot$ UW=1048·UW (we simplify calculations to a not cascode CMs). In the proposed implementation of 2-stage DAC the sum of UWs equals 70 ($\sum k_{1,x}$) + 85 ($\sum k_{2,x}$) + 25 + 10 (input transistors in the PMOS and NMOS CMs) = 190 i.e. is more than 5 times less. One of the disadvantages of the second approach is the increased number of branches in both DAC stages, resulting in slightly increased total current – an increase by ca. 5%.

The SAR algorithm is in the proposed circuit controlled by a simple digital block shown in Figure 5. Each BCELL, shown in Fig. 5(b), composed of a D-flip flop and several gates, controls a single bit.

III. Realization of the ADC in the CMOS 130 nm Technology

The circuit has been realized in the IHP CMOS 130nm technology and thoroughly verified by means of transistor level simulations performed in Spectre environment. Layout of the ADC is shown in in Figure 6. The overall digital part of the converter is located in one area (at the right side) to separate it from the analog part. Minimum transistor sizes have been selected on the basis of the analysis of the transistor mismatch, bearing in mind assumed ranges of the input signal. The optimal values are in this case (W/L) 4000/300 nm. We refer to the value W=4000 nm to as the Unit Width (UW). If

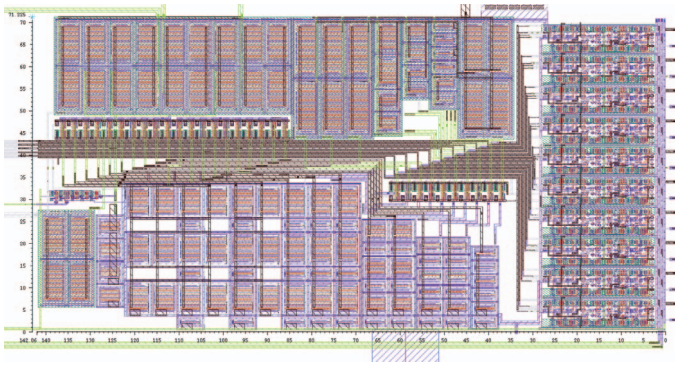

Fig. 6. Layout of the proposed SAR ADC realized in the IHP CMOS 130nm technology – area 0.01 mm^2 (sizes 142x71 μm).

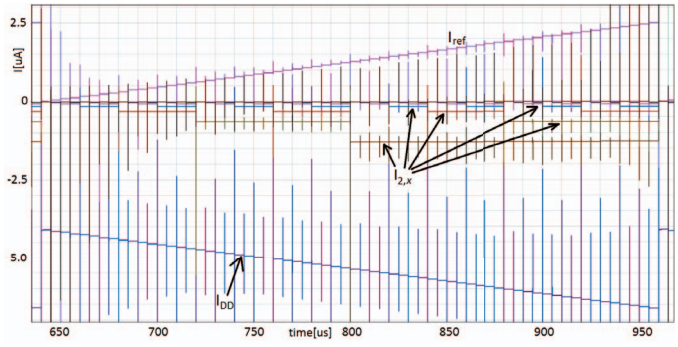

Fig. 7. Simulations of the DAC for the resolution of 6 bits (configuration P='0111111000', $I_{\rm tr} = 250$ nA, LSB $\sim$ 40 nA).

a 1-stage approach would be used the sizes of the width of largest transistor would equal 1024 · UW. The application of the 2-stage DAC approach allowed us to reduce this value to only 32 · UW, for 10 bits of the resolution.

Verification of the circuit has been performed in several steps, as presented in following subsections.

A. Open-Loop Simulations of the DAC

Since the DAC which provides the reference signal is the most important component of the SAR ADC, therefore in the first step we performs open loop tests of this block. We verified a general performance of the circuit (power dissipation vs. data rate) and the linearity of the input-output characteristic for the input signal varying over the overall input range. The upper range depends on the external current $I_{\rm tr}$. The scaling factor k (see Fig. 4(a)) equals 25, which means that the resolution ([nA]) of the LSB equals 1/25 of this current (for the resolution of 10 bits). The circuit was tested for the $I_{\rm tr}$ current varying in the range from 50 to 625 nA.

The proposed ADC is a flexible solution. The circuit can operate with various resolutions of the output signal, and additionally the user can decide which sections of the DAC will be used. This feature is controlled by a set of 10 bits, P. As a result, if for a reduced resolution a larger data rates are required we can use the MSBs sections instead of the smallest ones. Example results illustrating this feature are

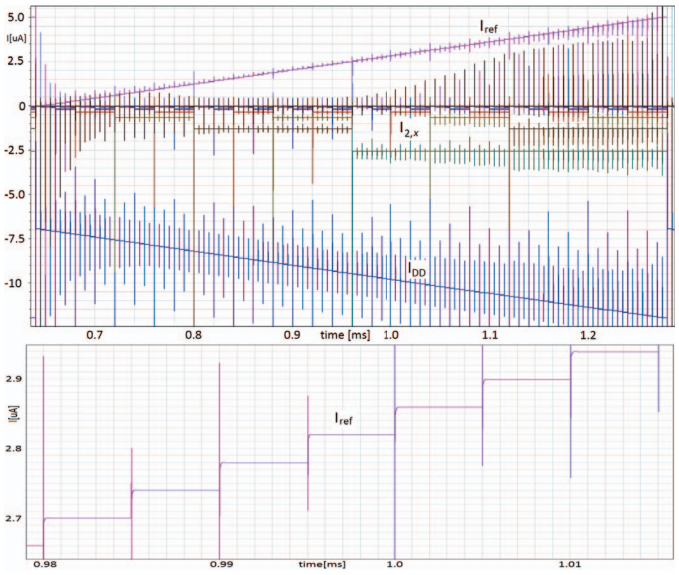

Fig. 8. Simulations of the DAC for the resolution of 7 bits (configuration P='1111111000', $I_{\rm tr} = 250$ nA, LSB $\sim$ 40 nA).

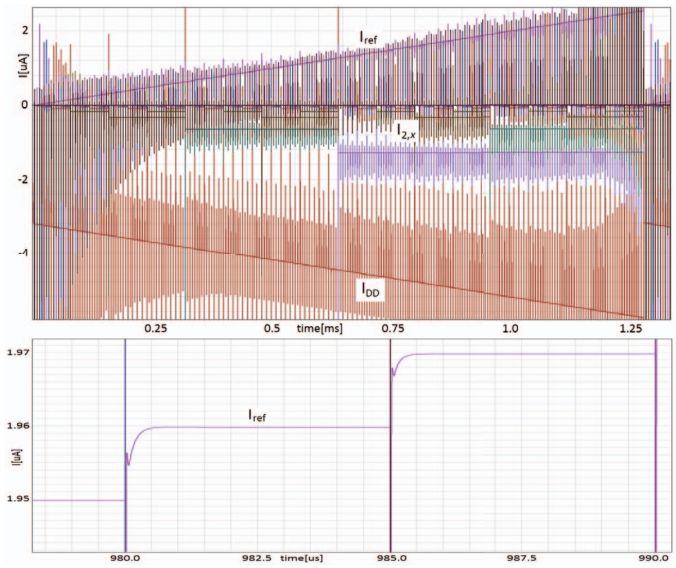

Fig. 9. Simulations of the DAC for the resolution of 8 bits (configuration P='0011111111', $I_{\rm tr} = 250$ nA, LSB $\sim$ 10 nA).

shown in Figs. 7, 8 and 9 for the resolutions of 6, 7 and 8 bits, respectively. In the first case we use sections 04 – 09 of the DAC, while sections 01 – 03 and 10 are switched off (P='0111111000'). In the second example we use sections 04 – 10 (P='1111111000'), while in the third example sections 01 – 08 are used (P='0011111111'). In the 1$^{\rm st}$ case the resolution of the LSB equals 40 nA, an average power dissipation equals 6.3 μW, and the conversion rate of the DAC equals 5 Mbits/s. In the 2$^{\rm nd}$ case the LSB resolution also equals 40 nA, an average power dissipation raises up to 11 μW, while the conversion rate remains at the level of 5 Mbits/s. In the 3$^{\rm rd}$ case the LSB resolution is reduced to 10 nA, which allows to

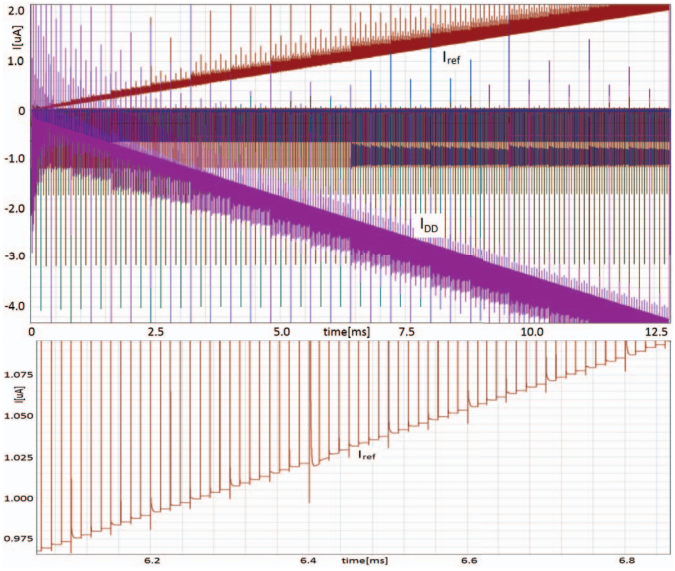

Fig. 10. Simulations of the DAC for the resolution of 10 bits (configuration P='1111111111', $I_{\rm tr} = 50$ nA, LSB $\sim$ 2 nA).

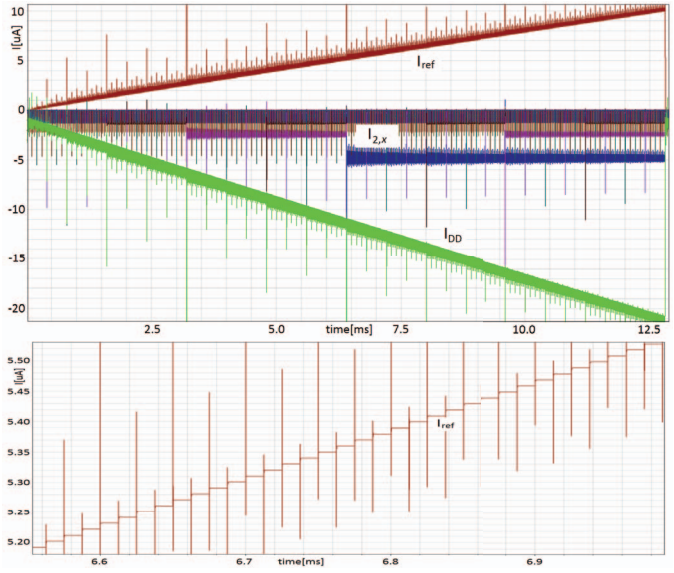

Fig. 11. Simulations of the DAC for the resolution of 10 bits (configuration P='1111111111', $I_{\rm tr} = 250$ nA, LSB $\sim$ 10 nA).

obtain the power dissipation of 7.44 μW but the conversion rate also reduces to 2 Mbits/s.

Figs. 10 and 11 present the results for the full scale resolution of 10 bits, for the $I_{\rm tr}$ current equal to 50 and 250 nA i.e. for the LSB resolution of 2 nA and 10 nA, respectively. The average power dissipation equals 2.64 μW and 13.2 μW in particular cases. For the $I_{\rm tr}$=50 nA case, the $I_{\rm ref}$ current (output of the DAC) usually achieves steady state within the period of 5 ns, but for some steps it takes even 20 ns. For $I_{\rm tr}$=250 nA the conversion rate slightly exceeds 1 MSample/s.

The carried out investigations show that the input-output characteristic of the DAC is in general linear. The simulated

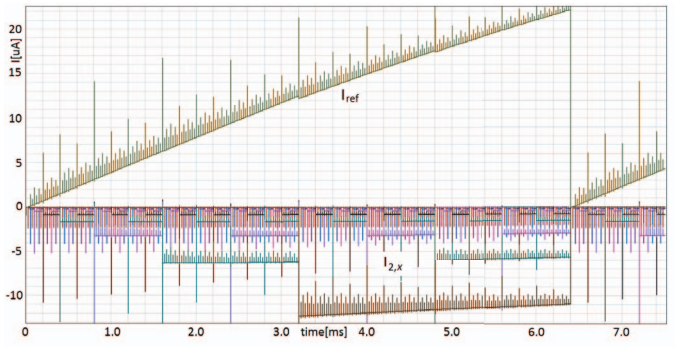

Fig. 12. Simulations of the DAC for the resolution of 8 bits (configuration P='1111111100', $I_{\rm tr} = 625$ nA, LSB 100 nA).

INL (integral nonlinearity) does not exceed 1 LSB. However this value will have to be confirmed in the laboratory tests, once the chip is fabricated.

The next step was to determine the maximum undistorted value of the input signal that can be processed by the ADC. For this purpose we performed tests shown in Fig 12 for $I_{\rm tr}$=650 nA, the resolution of 8 bits, and P='1111111100'. As we can observe the characteristic becomes nonlinear, but the reference current $I_{\rm ref}$ achieves the value of 22 μA. Probably this value can be achieved with a linear characteristic, but the $I_{\rm tr}$ current has to be reduced. This issue requires more investigations.

B. Closed-Loop Simulations of the Overall ADC

The ADC has been tested by means of transistor level simulations performed in the Spectre environment. We performed a typical corner analysis for different environment temperatures, supply voltages and transistor models. Fig 13 illustrates the convergence process of the SAR algorithm, for an example case of $I_{\rm tr}$=125 nA (LSB resolution = 5 nA), for the input current of 1500 nA, for temperatures of -20°C, +27°C and +70°C. The expected output value is 300 i.e. 0100101100. This value has been achieved for +70∘C degree, while for smaller temperatures the LSB is 1. However, the value of 300 is at the border between two codes, so the error is very small. A comparable situation is visible for different values of the input signal. The conversion time does not exceed 2 μs. In the comparison with the results presented in previous subsection for the DAC block, data rate of the overall ADC is smaller, but we have to remember that the comparator, realized in this case as a chain of NOT gates needs some additional time to settle. For larger values of the $I_{\rm tr}$ currents the expected data rate will be larger. It is worth to note that these results have been achieved for 10 bits of the resolution.

A brief comparison with other state-of-the art solutions of this type are presented in Table I. The Figure-of-Merit (FOM) has been defined as follows:

$$\mathrm{FOM} = P/(2^n \cdot f_{\rm S}) \tag{4}$$

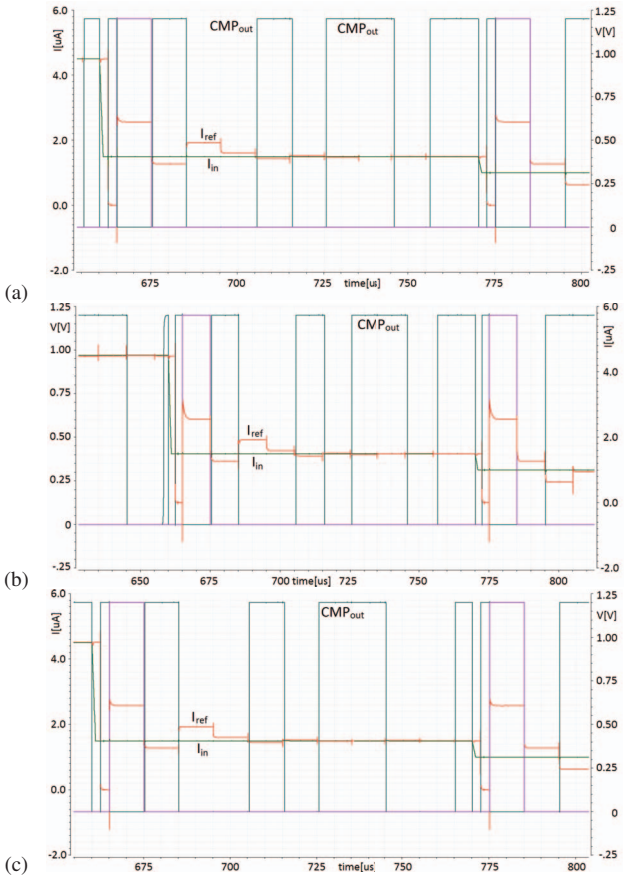

Fig. 13. Verification of the overall ADC – simulations of the convergence quality of the SAR algorithm for different temperatures: a) T=27°C, b) T=-20°C, c) T=70°C.

IV. Conclusions

In this paper, we presented a 10-bits current-mode SAR ADC designed in the IHP CMOS 130nm technology. The circuit is based on a 2-stage DAC that allows to reduce strongly the sizes of transistors used in this block. The resultant chip area equals only 0.01 mm^2 which makes the proposed ADC probably the smallest circuit of this type in the world. For a resolution of the LSB of 10 nA, and an average power dissipation of 13.2 μW, data rate for 10-bits conversion equals 0.55 MSamples/s. If the resolution is reduced to 8 bits and the MSB sections of the DAC are used, the sampling rate increases up to 2 MSamples/s. The presented results are obtained in the simulations, however, the chip fabrication is planned soon.

TABLE I
Comparison of low power and low chip area SAR ADCs

Ref. (Techn.)	Mode V / I	Res. bits	f_S [MSmpl./s]	P [mW]	A [mm^2]	FOM fJ/conv
[11] (130 nm)	V	10	50	0.826	0.0516	29
[12] (55 nm)	V	10	1	2.5	0.046	2441
[13] (130 nm)	V	10	1	0.147	ND	437
[14] (130 nm)	V	8	1	1.2	0.1	4687
[15] (90 nm)	V	8	10	0.026	0.054	12
[16] (130 nm)	V	8	0.1	0.0032	0.08	143
[17] (130 nm)	V	11	6.5	414	0.304	33
[18] (180 nm)	I	8	0.016	0.5	0.078	132
This work	I	10	0.55	0.0132	0.01	23.4

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