# 11 Analog-to-Digital Converters for Radiation Detection Electronics

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## 11.1 INTRODUCTION

The ability to peer into the human body is an essential diagnostic tool in medicine. Many of the imaging modalities, including computed tomography (CT) and SPECT/PET (single photon emission computed tomography/positron emission tomography) nuclear medicine techniques, are based on X-ray or γ-ray transmission and detection. In addition, radiation detection is used in numerous other fields, including high-energy physics, security, luggage scanning, and space applications. Despite their different principles of operation, there are numerous commonalities in the processing of signals received by these imaging detectors: signal amplification, filtering, multiplexing, and analog-to-digital conversion (ADC). The last step, A/D conversion, is essential, as gathered information is typically processed using digital signal processing algorithms.

The X-ray detection systems can be separated into direct- and indirect-conversion architectures. In the first case, a scintillator material is used to convert the photons to light that is then subsequently converted to an electrical signal using photodiodes, charge-coupled devices (CCDs), or CMOS (complementary metal-oxide semiconductor) imaging sensors. On the other hand, the direct-conversion concept, which is currently gaining popularity, converts photons directly into an electrical charge, which allows for a better image quality.

The block diagrams of two possible direct conversion schemes are shown in Figure 11.1. In the first approach, shown in Figure 11.1(a), the analog output signals of the charge-to-voltage (C/V) converters are serialized in the asynchronous multiplexer (MUX), stored in the first-in-first-out (FIFO) block, and then converted to a digital signal using a single high-performance ADC that usually is an external block in such systems. In the second approach, shown in Figure 11.1(b), each channel in the C/V or in the charge-to-current (C/I) converter is connected to a separate low-power and low-chip area ADC. Particular ADCs are active only when a given channel detects a photon. In this case, the analog FIFO block is not required, which simplifies the control circuitry. This additionally minimizes the number of copy operations at the analog side, which potentially increases the overall system performance.

The frequency content of different imaging signals covers different portions of the spectrum and signal bandwidths (BW), and can range from near DC to several kilohertz (kHz) and possibly up to a few megahertz (MHz). Some measured signals have higher amplitudes than others, and they range from a few microvolts (μV) to tenths of millivolts (mV). Both low-voltage operation and low-power dissipation are of great importance for these types of applications, because hundreds or thousands of imaging sensors have to be processed simultaneously. Low-voltage operation is demanded because it is desirable to use as few batteries as possible for size and weight considerations. Low current consumption is necessary to ensure no increase in sensor operating temperature and a reasonable battery lifetime for portable equipment.

Typical data acquisition systems have several performance limitations. They are normally based on ADCs with resolutions of between 8 and 14 bits, meaning that there is a relatively high dynamic range to deal with simultaneously strong noise disturbance signals (such as the 50/60-Hz power noise signal) of comparable magnitude. As CMOS technologies continue to evolve toward smaller geometries, new design techniques are being developed to improve the power efficiency of these ADCs while possibly reducing the silicon die area.

This chapter is devoted to the A/D converters used in medical imaging systems. We will briefly discuss ADC configurations that are suitable considering basic properties of flash, pipeline, and successive approximation (SAR) converters. A basic review of existing architectures indicates that the most power efficient converters are built using the SAR principle. For this reason, most of the material that follows will be devoted to SAR analog-to-digital converters. A review of existing SAR ADC solutions, new design techniques, and design examples will be presented and discussed. For other types of ADC architectures, readers can consult several books dedicated entirely to this topic [1, 28].

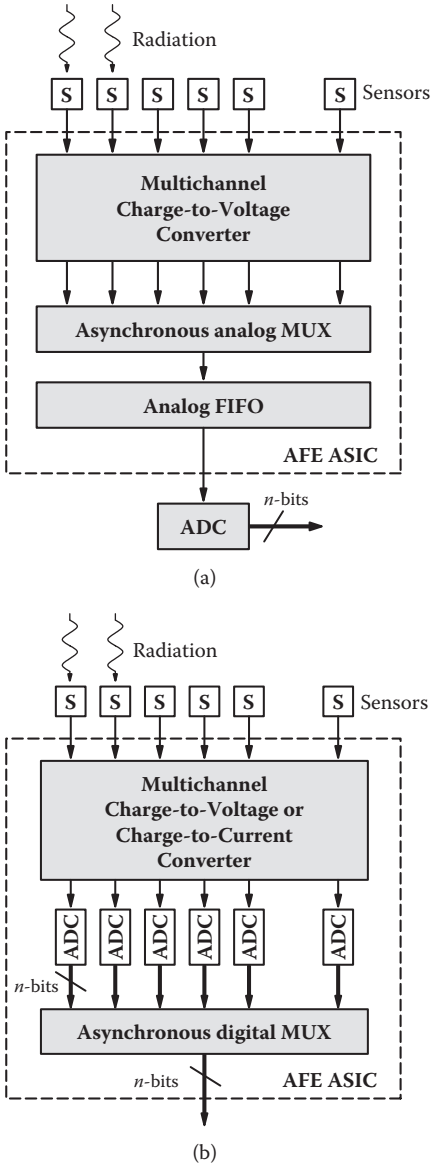


**FIGURE 11.1** Direct conversion architecture: (a) with analog FIFO structure and an external ADC; (b) without the analog FIFO block and a number of low-power and low-chip-area ADCs working in parallel, integrated with other blocks in the charge-to-voltage ASIC.

## 11.2 GENERAL CLASSIFICATION OF ADCS

Analog-to-digital converters can be classified as Nyquist rate ADCs and oversampled ADCs (sigma–delta). Sigma–delta ADCs are preferred for the highest bit resolutions; however, they demand very fast oversampling clocks, which makes them inherently

low-speed structures. Their clock generator has to be very clean, as the clock jitter has a direct influence on the obtained signal-to-noise ratio (SNR).

On the other hand, the Nyquist rate converters are typically used in applications that require lower data resolution and higher data rates. Nyquist rate converters usually have one of the following four architectures [1, 28]:

1. Flash
2. Pipeline
3. Folding–interpolating
4. Algorithmic and successive approximation register (SAR)

Taking into consideration such features as attainable data conversion rates, output data resolution, and power dissipation, particular converter architectures are preferred in different types of applications. SAR converters with only one comparator are simple structures with relatively low power dissipation, but as only one bit is calculated per one clock cycle, they are also relatively slow. In the applications where a high conversion rate is required, SAR ADCs put high demands on the comparator, which must be at least $n$ times faster than comparators in flash converters for the same data rate, where $n$ is the resolution of the output data. SAR converters require a very good calibration of the digital-to-analog converter (DAC), since the DAC accuracy has a direct influence on linearity of the input–output characteristic. In SAR converters, all bits are calculated under equal conditions using the same comparator. Hence, the offset of the comparator does not have influence on the linearity of the input–output characteristic. However, the offset can shift the characteristic by a constant DC value. To achieve a short conversion time, several SAR ADCs can be time interleaved; however, in this case, power budget and nonuniformities of ADC characteristics become more critical.

In flash ADCs, all bits are calculated in parallel, which makes this type of conversion potentially the fastest of all approaches. The state-of-the-art converters of this type implemented in a standard CMOS process operate with sampling rates of up to several gigahertz (GHz) [62–64], while the rates realized in SiGe technology can be up to several dozen gigahertz [65]. In this architecture, offset compensation is very important, since different offsets of comparators operating in a thermometer-type conversion have a direct influence on the differential nonlinearity (DNL) of the input–output characteristics. The price for a high resolution and a fast conversion is very high power dissipation, as the number of comparators is equal to $2^{n-1}$. For this reason, flash converters are used in high data rate applications that accept low resolutions, typically in the range of 3 to 6 bits, and where power dissipation is of a secondary importance. Their application in medical imaging is virtually nonexistent, besides PET systems, where they are typically used as a low-resolution component in time-to-digital schemes [67, 68].

Taking power dissipation and data rate criteria into account, SAR and flash ADCs can be viewed as two extreme cases [57], while other ADC architectures such as pipelined and folding–interpolating can be seen as the intermediate solutions. The last two types of converters usually are designed for higher resolutions (14–20 bits) [61], but present a trade-off of the number of comparators, the conversion rate, and

the power dissipation. For example, low-resolution flash ADCs are used in particular $k$-bit stages of pipelined ADCs. This minimizes the total number of comparators when compared with pure flash solutions, but conversion of each data point requires several clock cycles. In general, pipelined and folded–interpolated architectures have much more complex structure than SAR converters, since they require a more complex control block [61].

Figure 11.2 shows a comparison of existing converter solutions in terms of data rate versus dissipated power for selected converters of different types [2–27, 31–60, 62–64]. All presented results have been normalized to 8 bits of resolution and with respect to $V_{DD}^2$, where $V_{DD}$ is the power supply level. As can be observed, the dissipated power correlates well with the sampling frequency, as expected.

Each group of converters is clustered in one area of the plot, although these areas slightly overlap. The placement of particular groups corresponds to the previous description. The most flexible architecture in terms of the power dissipation and the sampling frequency is the first group. Algorithmic-SAR converters usually are designed for low sampling frequencies and low power dissipation, although time-interleaved architectures have recently been gaining popularity [11, 44–48]. These converters use relatively slow SAR blocks working in parallel. Due to the low number of comparators that is equal to data resolution, $n$, instead of $2^n$ as in flash

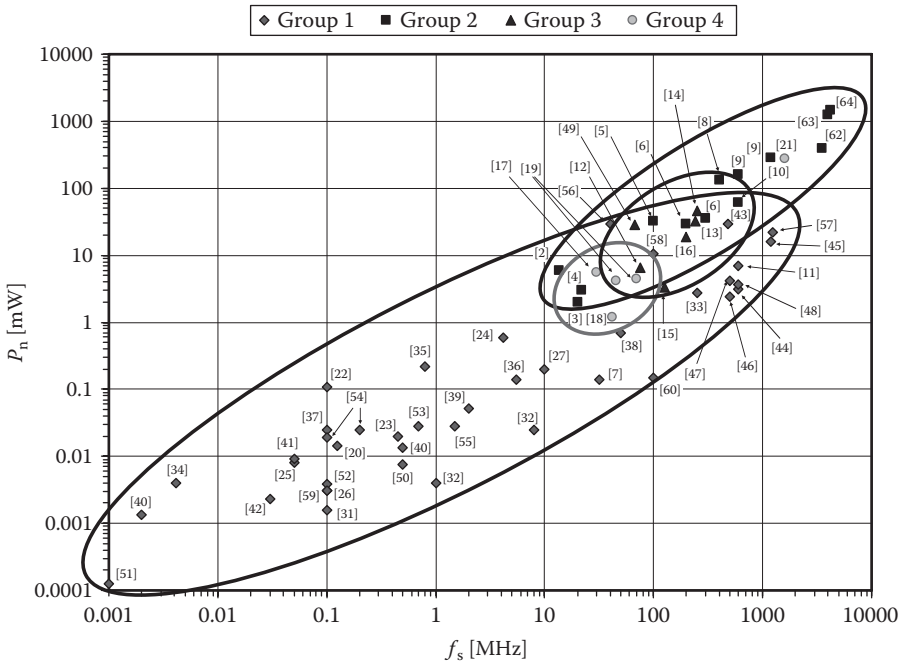


**FIGURE 11.2** Performance comparison of four groups of ADCs: Group 1, algorithmic and SAR; Group 2, flash; Group 3, pipelined; Group 4, folding and interpolating. Normalized power with respect to $V_{DD}$ = 1 V. (Based on Dlugosz and Iniewski [32]. © 2007 by Hindavi Publishing. With permission.)

ADCs, these converters can effectively compete in terms of sampling frequencies, simultaneously dissipating much less power. Comparing, for example, converters [9] with [45] and [8] with [46], we see that power dissipation differs by as much as one order of magnitude for similar sampling frequencies.

## 11.3 SAR PRINCIPLE OF OPERATION

A typical classic SAR converter contains four main components, as shown in Figure 11.3, i.e., the sample-and-hold element (S&H) that is used to acquire the input signal, a comparator, a digital-to-analog converter (DAC), and the control-logic circuitry that controls the calculation scheme.

In SAR ADC, a binary search algorithm is used in the conversion of the analog signal into its digital representation. This algorithm consists of several steps. Initially after resetting the logic circuitry and DAC circuit, the most significant bit (MSB) is set to digital 1. The DAC block supplies the analog equivalent signal of this code into the comparator circuit for comparison with the sampled input signal that is stored in the S&H circuit. Depending on which signal is larger (input or reference), the comparator either resets or maintains this bit. In the next step, the second bit is set up to a digital 1, and the DAC block supplies a new value for the reference signal. This binary search is performed for all bits until the least significant bit (LSB) is tested.

SAR converters usually are implemented using the voltage-mode charge-redistribution architecture shown in Figure 11.4. The most characteristic block in this approach is a charge-scaling DAC, which consists of an array of individually switched binary-weighted capacitors. These capacitors also serve as an S&H memory element. A whole conversion cycle performed in this converter consists of three initial steps followed by a conversion algorithm that is then performed in $n$ phases.

Each conversion cycle starts with discharging of the capacitor array. A good technique is to discharge capacitors to the offset voltage of the comparator instead of the ground, as this enables automatic offset cancellation. In the next step, free terminals of all capacitors are switched to the input voltage $V_{in}$, while the common terminal is switched to the ground (acq = 1 and sar = 0). The amount of charge that is switched to the particular capacitors is equal to their capacitance times the input voltage. In the third step, the common terminal is disconnected from the ground and remains connected to the comparator's negative input, while all free terminals are connected to the ground ($b_i = 0$, for $i = 1, \ldots, n$). As a result, the comparator input voltage

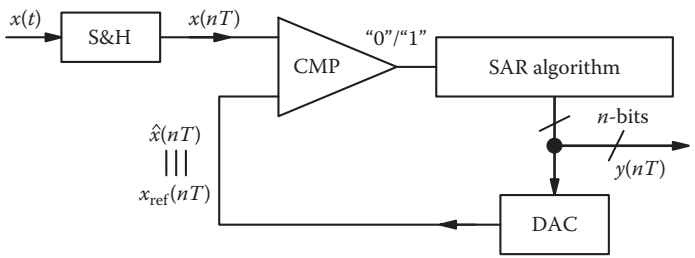


**FIGURE 11.3** A schematic block diagram of the successive approximation ADC.

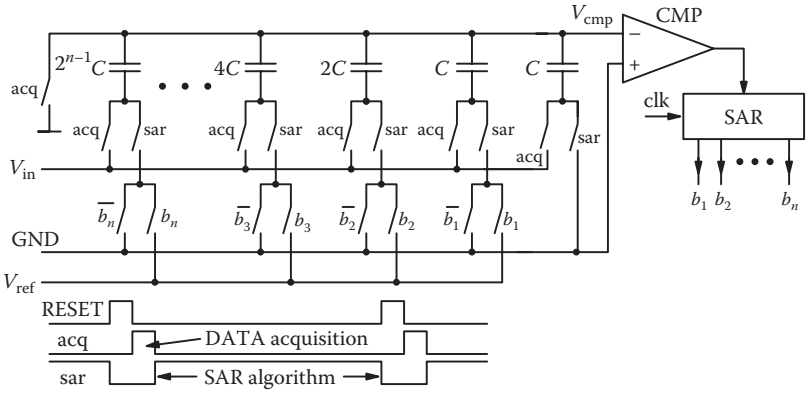


**FIGURE 11.4** Schematic diagram of the charge-redistribution SAR ADC architecture.

equals the negated value of the input signal. Finally, the SAR conversion algorithm starts in the fourth step.

In the following $n$ clock cycles, particular binary-weighted capacitors, from MSB to LSB, are switched to the reference voltage $V_{ref}$ that corresponds to the full-scale voltage ($V_{FS}$) range of the ADC. First, the MSB capacitor is switched to $V_{ref}$ ($b_n = 1$). As a result, the comparator's negative input voltage becomes $-V_{in} + V_{ref}/2$. Depending on the comparator's output, the first capacitor remains connected to $V_{ref}$ voltage or is switched again to ground. In the next clock cycle, the second capacitor in the array is connected to $V_{ref}$, and the comparator's input becomes equal to $-V_{in} + V_{ref}/2 + V_{ref}/4$ or to $-V_{in} + V_{ref}/4$, depending on the previous comparison result. This sequence is repeated for all bits, so the comparator-negated input voltage can be expressed as follows:

$$V_{cmp} = -V_{in} + V_{ref} \sum_{i=1}^{n} \frac{b_i}{2^{n-i+1}} \tag{11.1}$$

SAR converters can also be implemented using current-mode circuits. In this case, the DAC block is realized as a multi-output current mirror, with particular output transistors being binary weighted. In current-mode SAR converters, the initial phase is shorter compared to charge-redistribution solutions. In this case, sampling of the input signal in the S&H element can be performed in parallel with resetting the logic circuitry. The conversion algorithm is similar to that performed in the voltage-mode approach. Particular bits set up the value of the reference current, which is compared with the input signal in the current-mode comparator.

Current-mode SAR converters have several advantages over charge-redistribution architectures. A shorter initial phase is one such advantage. Another one is the very small amount of energy consumed during the calculation of a single bit. Currents that flow in the current-mode DAC must charge only parasitic capacitances, in particular transistors, which may be even several orders of magnitude smaller than capacitances in charge-redistribution converters. As a result, current-

mode converters are more power efficient and potentially faster. An additional advantage is very small chip area, since the DAC block in this case does not contain large capacitors.

The disadvantage of current-mode SAR converters is lower resolution than in charge-redistribution solutions. Since the DAC block in this case is realized as the current mirror, the transistor-matching problem occurs. This problem, which has an influence on the linearity of the input–output characteristics, becomes especially important for small currents and small power supplies when transistors work in a weak inversion region. Since the DAC block in charge-redistribution converters is implemented using capacitors whose matching does not depend on the value of supply voltage, this problem is less insignificant in this case.

## 11.4 SAR VERSUS FLASH ADC

An exact comparison of SAR and flash converters has been performed by Ginsburg and Chandrakasan [46] on the basis of developed analytical energy models. These models enable the selection of a given architecture for a given application in cases where power dissipation is the main criterion. In flash architectures, energy is consumed mostly by comparators, while in SAR converters, all building blocks described earlier must be considered in the energy model. In SAR ADCs, particular energy components have different distributions over the converter's resolution, as shown in Figure 11.5.

In a comparator with a two-stage preamplifier, energy varies almost linearly with the converter's resolution. The comparator must make the proper decision even when both input voltages differ insignificantly. When the converter's resolution increases,

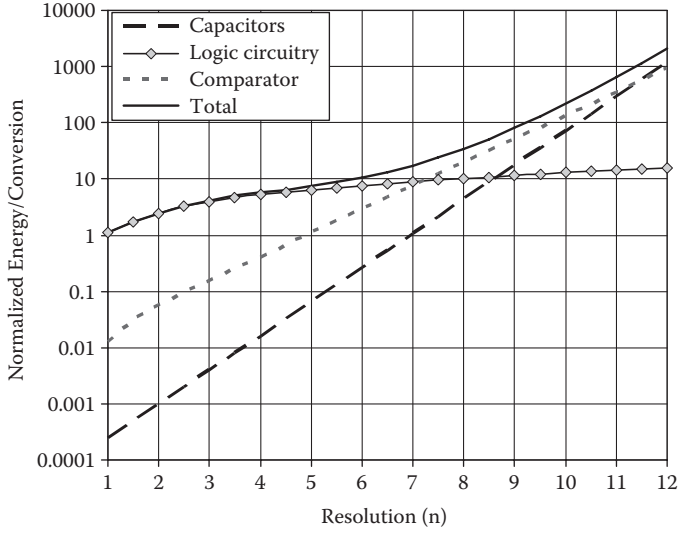


**FIGURE 11.5** Energy versus resolution in SAR converters for particular building blocks such as comparator, DAC, and control logic. (From Ginsburg and Chandrakasan [46]. © 2007 by IEEE. With permission.)

then the minimal difference between inputs decreases, and preamplifiers must have higher gains to ensure the appropriate settling time of the comparator.

Energy consumed in the logic circuitry increases only moderately with the resolution, as each algorithm step requires almost the same control block. The moderate increase that is visible in Figure 11.5 is due to the different dimensions of switches in particular stages. In cases of larger capacitors, the on-resistance of switches must be smaller to keep the settling time constant in all stages. Energy that is consumed by the capacitor array increases exponentially with the converter's resolution, which is due to the exponential growth of capacitance in the following DAC stages.

Models presented by Ginsburg and Chandrakasan [46] take into consideration the influence of the full-scale input voltage ($V_{FS}$) on the energy of the converter. When the value of $V_{FS}$ increases in a SAR converter, then a bigger charge is fed to the capacitors in each conversion cycle. On the other hand, a higher value of $V_{FS}$ minimizes the gain requirements of preamplifiers in the comparator, resulting in a lower level of energy consumed by this element. The decrease of energy consumption in the comparator compensates the increase of energy in the capacitors. As a result, in SAR converters, energy varies only moderately with $V_{FS}$. In the case of flash converters, where energy is consumed mostly by comparators, higher values of $V_{FS}$ enable significant improvement.

Published models show that each converter is suitable for different values of parameters. For example, when the resolution is higher than 4 bits, then for a $V_{FS}$ that is equal to 300 mV, SAR converters exhibit better efficiency than flash converters, as shown in Figure 11.6(a) [46]. For a given resolution when $V_{FS}$ is higher than some threshold value, then flash architecture attains better power efficiency. This is illustrated in Figure 11.6(b) for an example resolution of 5 bits.

## 11.5 STATE OF THE ART IN SAR ADC DESIGN

SAR converters are usually designed for resolutions between 8 and 10 bits, although higher resolutions up to 14 bits are also reported [37, 43]. Higher resolutions require special techniques that enable a proper calibration of DAC to ensure a high linearity of the input–output characteristic. For example, in the converter described by Hesener et al. [43], the capacitor array is realized as a cluster of small unity capacitors with redundancy in the number of these unity capacitors. Configuration of the array is controlled by an additional logic circuit, which at each algorithm stage calculates the required capacitors values and programs the capacitor array. This mechanism allows for the correction of capacitor mismatch, but makes the structure more complex and increases both the chip area and power dissipation that is, in this case, the highest of all SAR converters presented in Figure 11.2.

Most of the reported SAR ADCs have been designed as voltage-mode architectures. In the classic charge-redistribution scheme, larger resolutions are difficult to attain, as capacitance values for each additional bit must be doubled. This doubles also the power dissipated in the capacitor array during data acquisition. Minimizing the value of the unity capacitor brings no effect, since it worsens matching between capacitors.

An example implementation of classic charge-redistribution converter has been described by Sauerbrey, Schmitt-Landsiedel, and Thewes [34]. This 9-bit converter

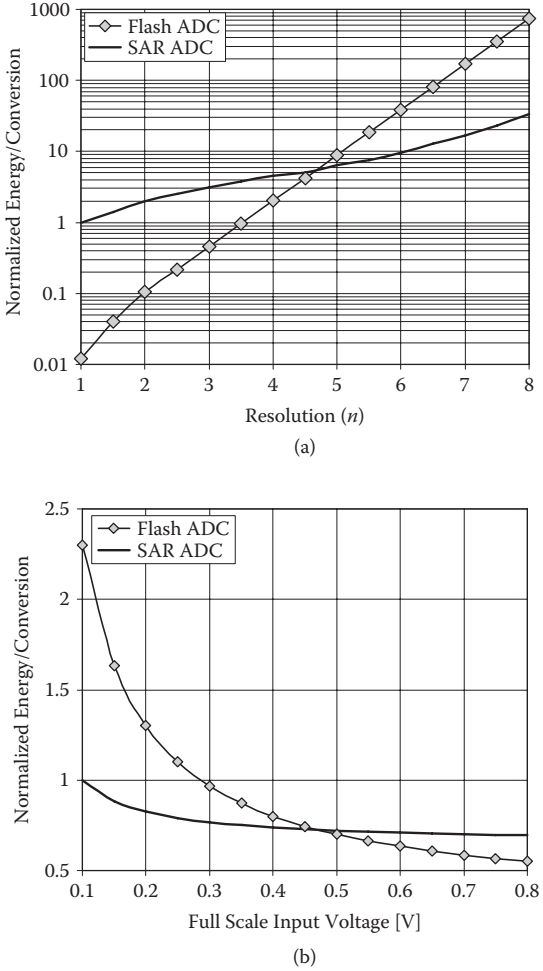


**FIGURE 11.6** A comparison of ADC for SAR and flash converters: (a) energy versus resolution for $V_{FS} = 300$ mV, (b) energy versus full-scale input voltage for resolution of 5 bits. (From Ginsburg and Chandrakasan [46]. © 2007 by IEEE. With permission.)

for the sampling frequency of 150 kHz dissipates power of 30 μW from a 1-V power supply, and for 4.1 kHz dissipates power of 0.85 μW from 0.5 V. In this case, the unity capacitor has capacitance that is equal to 20 fF, while the biggest capacitor has capacitance of 5 pF, which makes the overall capacitance in the circuit larger than 10 pF. For 12 bits of resolution, the overall capacitance in the circuit would be larger than 80 pF. This would limit the possible sampling frequency by several times for a given value of the power dissipation. An additional problem related to the capacitor array is the large chip area of the array that, in this case, is equal to about 70% of the overall chip area. All these problems show practical limitations of the classic charge-redistribution architecture. To overcome these problems, various optimization techniques are used.

### 11.5.1 Optimization of the Capacitor Array

One of the possibilities to minimize power dissipation is minimizing the value of the unity capacitor, but this technique increases the matching error. As a result, it creates a trade-off between power dissipation and the linearity of the converter. This problem can be solved in several ways. For example, in the 8-bit converter reported by Scott, Boser, and Pister [26], a careful design of the capacitor array enabled a high linearity of DAC for a small unity capacitor with a capacitance of only 12 fF and an overall capacitance of 3 pF. This converter has also been designed using the classic charge-redistribution architecture, but due to several optimization techniques, power dissipation (3.1 μW) is in this case almost one order of magnitude smaller than in the case of a converter reported by Sauerbrey, Schmitt-Landsiedel, and Thewes [34] for the same sampling frequency of 100 kHz. Poly–poly capacitors have been used with top plates used as common plates. This technique allows for the minimization of the parasitic capacitance at the comparator input. The dummy capacitors have been placed around the capacitor array, and they improve matching between capacitors and the linearity of the DAC. The other interesting technique used in this converter is placing a grounded metal shield over the poly–poly capacitors and then routing the capacitors above this shield. This technique makes the capacitors array insensitive to routing parasitics, which protects the array against systematic matching errors. The resultant DNL and INL (integral nonlinearity) parameters are kept on a very low level of ±0.25 LSB.

Another optimization method of the capacitor array that has gained some popularity in recent years takes advantage of the split-array technique [40, 52, 66]. In this technique, instead of using the binary-weighted capacitor array—as in the converters reported by Scott, Boser, and Pister [26] and Sauerbrey, Schmitt-Landsiedel, and Thewes [34]—an additional attenuation capacitor, $C_{att}$, divides the capacitor array into two subarrays responsible for calculation of LSBs and MSBs, respectively, as shown in Figure 11.7. When capacitance of the attenuation capacitor has a value that satisfies the following equation:

$$C_{att} = C\frac{\sum(\text{LSB capacitors})}{\sum(\text{MSB capacitors})} \tag{11.2}$$

then the resultant values of LSB capacitances that the comparator sees at point A are smaller by a factor of $2^i$, where $i$ is the number of LSB capacitors (excluding a dummy capacitor $C_d$).

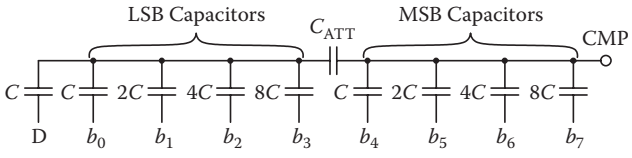


**FIGURE 11.7** A split-capacitor array that enables reduction of the ratio between the largest and smallest capacitors in a DAC block. (From Abdelhalim, MacEachern, and Mahmoud [40]. © 2007 by IEEE. With permission.)

This technique allows a significant reduction of the spread between the smallest and the largest capacitors in the array, maintaining capacitors in MSBs that are relatively small. In the converter described by Abdelhalim, MacEachern, and Mahmoud [40], this allowed an increase of the unity capacitor, which improved matching. The unity capacitor has, in this case, a value of 211 fF, whereas the largest capacitor in the circuit is equal to only 1.56 pF (compared to 20 fF and 5 pF, respectively, in the capacitor described by Sauerbrey, Schmitt-Landsiedel, and Thewes [34]). The value of the attenuation capacitor $C_{att}$ is equal to 225 fF. The smallest capacitor in the LSB area has a value of only 13 fF. These values are similar to those in the converter presented by Scott, Boser, and Pister [26], and the resultant sampling frequencies and power dissipation are also similar. For example, this converter dissipates power of 8.5 μW for 500 kS/s and less than 1 μW for 60 kS/s. In the converter described by Agnes et al. [52], the unity capacitor is 120 fF, while the largest one is equal to 3.8 pF.

### 11.5.2 Optimization of the Comparator

Improvement in SAR ADC's performance is also possible through the optimization of the comparator. The energy model introduced by Ginsburg and Chandrakasan [46] shows that offset of the comparator has a direct influence on the effective number of bits (ENOB), i.e., on the output data resolution. The optimization techniques, in this case, rely on minimizing the offset or increasing the gain of preamplifiers in comparators, which enables offset compensation. In the converter reported by Verma and Chandrakasan [31], several optimization techniques have been used. One of them introduces an offset-compensating regenerative latch into the comparator, which enables a decreased gain of the preamplifier, improves the power-delay product (PDP), and decreases the propagation delay in the comparator. The settling time has been additionally improved by introducing the self-timing technique. As a result, resolution of 12 bits is possible in this converter for sampling frequency of 100 kHz and power dissipation on the level of 25 μW. For comparison, in the converter reported by Sauerbrey, Schmitt-Landsiedel, and Thewes [34], an ENOB of 9 bits has been achieved for 30 μW of power.

The other offset correction technique has been introduced in the converter design reported by Abdelhalim, MacEachern, and Mahmoud [40]. The comparator scheme is shown in Figure 11.8. In this block, during the sampling phase, both comparators' terminals are switched to $V_{SS}$, the switch controlled by the RST signal is closed, and the gates of transistors M9 and M10 are on the common potential, which is equal to $V_{DD}/2$ plus an offset voltage. This value is stored across the capacitor $C_{off}$. During the conversion phase, the switch is opened and the output signal from the first stage is compared with the signal that is stored across capacitor $C_{off}$. This technique allows for a reduction of the offset of more than 60%. It is worth noting that this converter can operate in a relatively wide range of the supply voltage between 0.36 and 0.8 V. When operating with the small value of supply, the converter dissipates only 230 nW for the sampling frequency equal to 20 kHz. This is the smallest power dissipation reported so far. This result is much better than in the converter reported by Sauerbrey, Schmitt-Landsiedel, and Thewes [34], where for the supply voltage of 0.4 V and the power dissipation equal to 280 nW, the sampling frequency is equal to only 600 Hz.

Another solution, which can be referred to as nonconventional, has been proposed by Agnes et al. [52]. This SAR ADC uses a time-domain comparator that allows for realization of a power-efficient converter. The comparator is shown in Figure 11.9. It consists of two voltage-to-time (V2T) converters and a logic circuit. Transistors

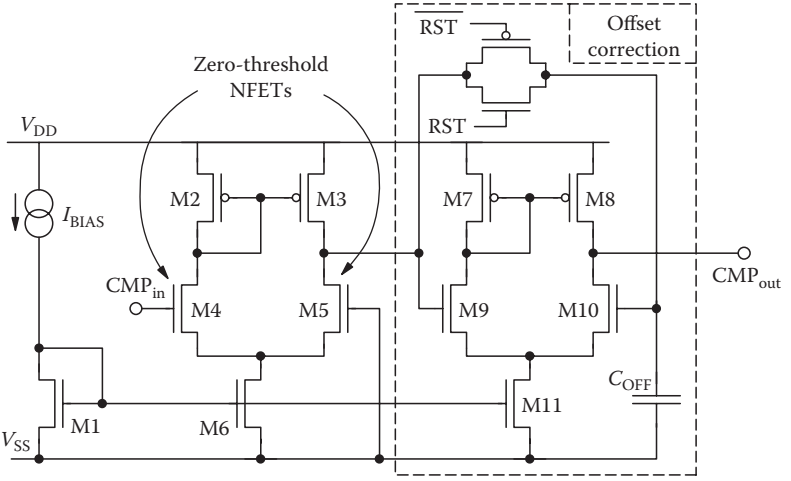


**FIGURE 11.8** A comparator with offset correction used in a converter. (From Abdelhalim, MacEachern, and Mahmoud [40]. © 2007 by IEEE. With permission.)

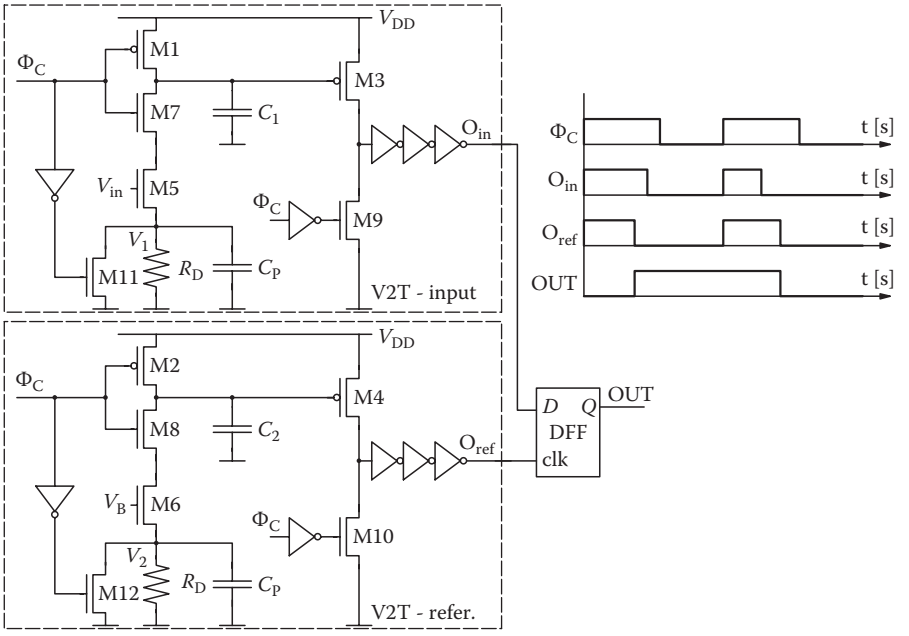


**FIGURE 11.9** Time-domain comparator. (From Agnes et al. [52]. © 2008 by IEEE. With permission.)

M1 and M2 in V2T blocks charge the nominally equal capacitors C1 and C2. When the voltages across the C1 and C2 capacitors cross the threshold voltages of M3 and M4 transistors, the chains of inverters switch, producing two logical 1 signals with different delays that depend on values of the input voltages. A DFF (D-type flip-flop) circuit at the output, which serves as a time comparator, determines which V2T is faster, i.e., which logical 1 occurs first. The comparator operates with less than 1 μW of power at 1-V supply and enables sampling frequency of 1.4 MHz with 0.2-mV sensitivity. Comparing this ADC with a solution reported by Scott, Boser, and Pister [26], the sampling frequency is, in this case, more than one order of magnitude higher for a similar power dissipation of 3.8 μW. The resolution of 10 bits is also higher in this case. The possible offset in the comparator is, in this case, due to a mismatch between transistors used in both V2T blocks. In the case when both input voltages are equal, the mismatch causes the currents that charge the capacitors C1 and C2 to differ slightly. The offset can be corrected by adjustment of the bias voltage $V_B$.

## 11.6 DESIGN EXAMPLE OF 8-BIT CURRENT-MODE SAR

Although most algorithmic-SAR converters have been designed using the charge-redistribution approach described earlier, in the case of low-power, low-chip area and low-to-moderate sampling frequency applications, current-mode algorithmic or SAR converters are gaining popularity [20, 23, 27, 29, 32, 60]. Considering direct-conversion architecture with multiple ADCs, shown in Figure 11.1(b), a chip area of a single ADC is the parameter as important as the energy consumption. A small area can be achieved only in current-mode SAR ADCs, which do not require large capacitors in DAC. As a result, the die size of current-mode ADCs can be 20–50 times smaller than that of voltage-mode converters. For example, the converter described by Agnes et al. [52] occupies an area of 0.24 $mm^2$, while an example current-mode converter reported by Yang and Van der Spiegel [60] occupies an area of only 0.005 $mm^2$, and another converter described by Dlugosz and Iniewski [32] occupies an area of 0.009 $mm^2$.

An example is the current-mode SAR converter shown in Figure 11.10 [32]. It consists of the analog circuitry responsible for signal conversion and the control-logic block. In this case, both analog and digital parts are powered from separate power supplies to enable power-down modes and to reduce digital-to-analog noise cross talk.

This converter derives its essence from the typical integrating current comparator realized on the CMOS inverters. This circuit converts an input current $I_{in}$, which is obtained by using a current-mode sample and hold (S&H) element. The input current is compared in each approximation step with a reference current $I_{ref}$, which is the output of the current-mode DAC and can be expressed as

$$I_{ref} = (b_n \cdot 2^{n-1} + b_{n-1} \cdot 2^{n-2} + \ldots + b_2 \cdot 2 + b_1) \cdot I_{tr} \tag{11.3}$$

where $I_{tr}$ is a biasing current. The differential current, $I_c$, between $I_{in}$ and $I_{ref}$ ($I_c = I_{in} - I_{ref}$) changes the voltage across the input gate-to-source capacitances of the first inverter

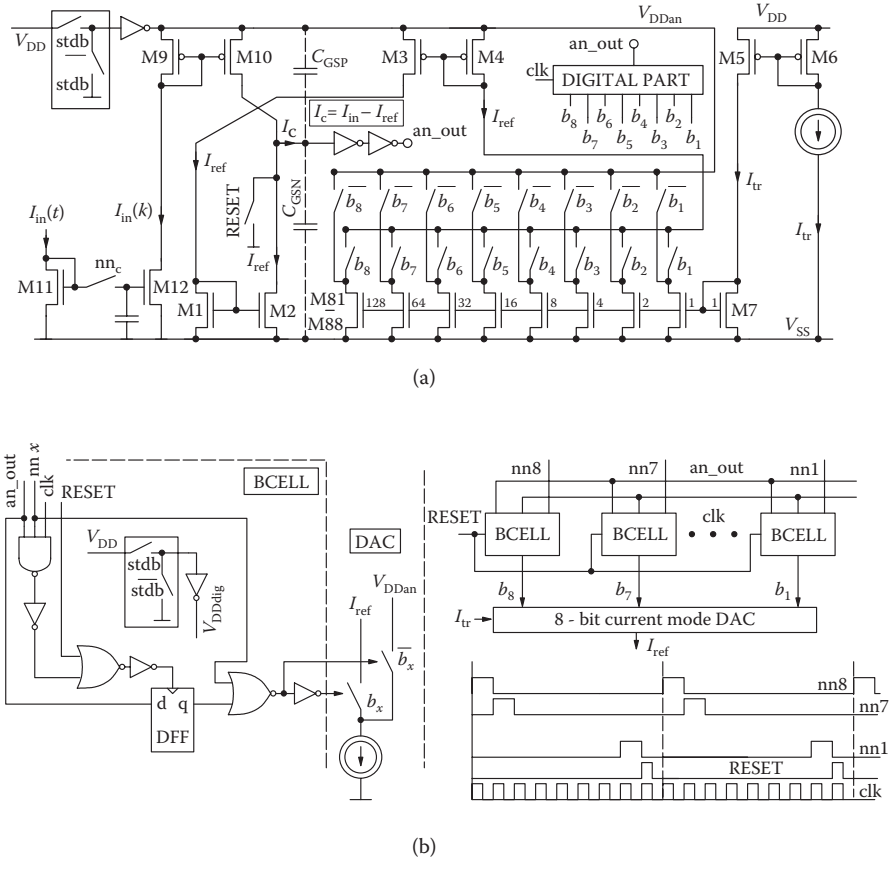


**FIGURE 11.10** A block diagram of an example current-mode SAR ADC with an implemented standby mode: (a) analog part and (b) digital part. (From Dlugosz and Iniewski [32]. © 2007 by Hindavi Publishing. With permission.)

(integrating comparator). The digital output signal ($V_{an\_out}$) and clock (clk) control the logic circuitry that sets bits $b_1 - b_n$, using a successive approximation algorithm.

Converter functionality is illustrated in Figure 11.11 for operation at 1-MHz sampling frequency and $I_{tr}$ current equal to 1 nA. The waveform depicts $V_c$ voltage at the input of the first NOT gate of the comparator during the SAR operation. The transistor's dimensions of the first NOT gate (comparator) were selected as minimal to minimize gate-to-source capacitance ($C_{GS}$) in order to obtain the highest possible speed of this circuit.

One of the advantages of the proposed ADC is that good matching between transistors in pairs M1-M2, M3-M4, M5-M6, M7 and M81-M88, M9-M10, M11-M12 is not critical, because any mismatch in these pairs can be compensated by adjusting the $I_{tr}$ current during device calibration. However, sufficiently good matching between transistors M81-M88 is important, as it can substantially affect the linearity of the ADC.

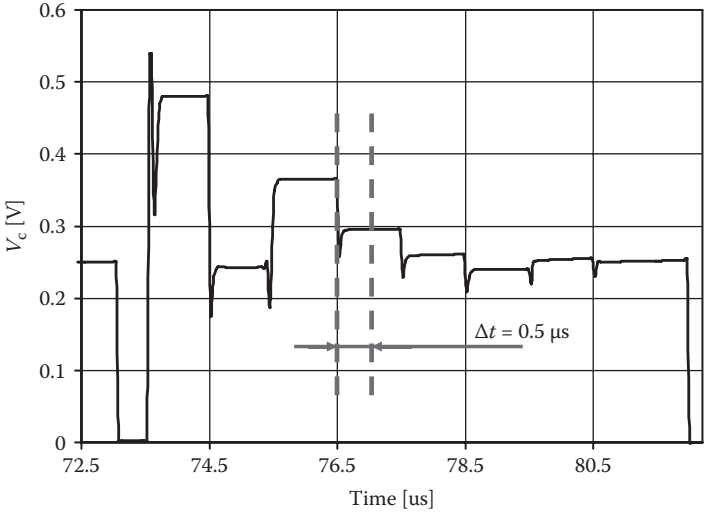


**FIGURE 11.11** Successive calculation of the output bits for an example input current $I_{in}$ = 211 nA sampled with $f_s$ = 1 MHz, and for $I_{tr}$ = 1 nA. $V_c$ depicts voltage of the current comparator. (From Dlugosz and Iniewski [32]. © 2007 by Hindavi Publishing. With permission.)

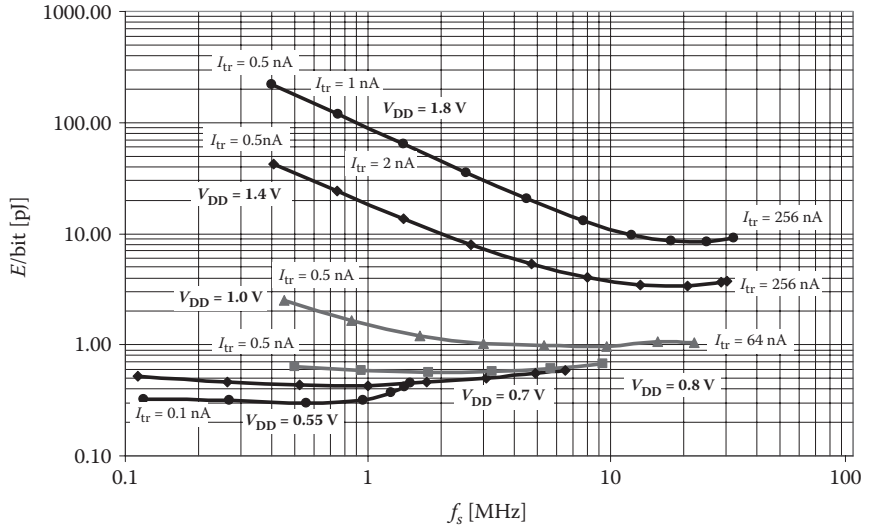


**FIGURE 11.12** Energy per calculated bit versus sampling frequency for different values of supply voltage $V_{DD}$.

The described converter has one important characteristic: Adjustment of the $I_{tr}$ current and the supply voltage $V_{DD}$ allows for the flexible regulation of power consumption and sampling frequency over a wide range. Figure 11.12 illustrates energy consumed per 1 bit versus the sampling frequency for different values of power supply ($V_{DD}$). As can be observed, the optimal region of operation depends on the $V_{DD}$ value.

The converter power is dissipated by the comparator, by the control logic block, and by the DAC. Power of the control-logic block does not exceed 10% of the overall power dissipation and increases linearly with the sampling frequency. The percentage contribution to the overall power dissipation in the case of comparators, implemented here as an inverter, depends on voltage supply. In CMOS gates working in standard digital applications, transition states between the logical values 0 and 1 are short, and energy lost during switching is relatively low. Both the input and the output voltages of the first inverter in the comparator are close to the $V_{DD}/2$ point, especially when, during the following algorithm steps, the reference signal becomes close to the input signal, as shown in Figure 11.11. When the supply voltage is low, then both transistors in the inverter operate in the weak inversion, and current that flows in the inverter can be neglected. Otherwise, when $V_{DD} > V_{TH\_pMOS} + V_{TH\_nMOS}$, then current flowing in the inverter becomes significant for the output voltage in the midpoint between $V_{DD}$ and $V_{SS}$. For small supply voltages, power dissipation linearly increases with the sampling frequency, and energy per bit is approximately constant. When supply voltages are high, then power dissipated in the comparator becomes a dominant component, especially for small input and reference currents. In this situation, power dissipated in DAC can be neglected. For small sampling frequencies and high supply voltages, power dissipation is almost constant, and energy per 1 bit increases linearly when sampling frequency decreases.

Each curve in Figure 11.12 has a minimum, i.e., the most optimal value of energy per conversion step. Figure 11.13 illustrates placement of these optimum values for particular values of the power supply vs. sampling frequency. The best parameters are attained for moderately low supply voltages around 1 V. For this supply, the optimum parameters are obtained for the sampling frequency of 10 MHz.

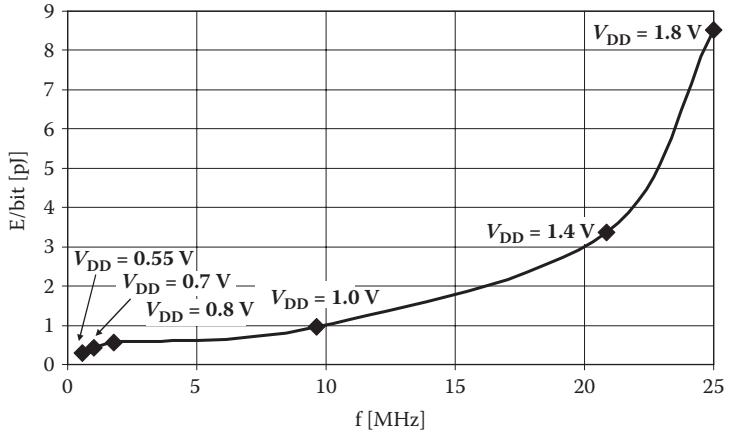


**FIGURE 11.13** Optimal energy per 1-bit versus sampling frequency for given supply voltages $V_{DD}$.

## 11.7 OPTIMIZATION TECHNIQUES IN CURRENT-MODE SAR ADCs

A problem that must be considered in the current-mode SAR ADC is transistor mismatch, which requires very precise DAC calibration, as described by Yang and Van der Spiegel [60]. The mismatch problem is especially important when transistors operate in the weak inversion region at small power supplies. In such converters, DAC is implemented as a multi-output current mirror with binary-weighted transistors, and in this case, mismatch has a direct influence on the differential nonlinearity (DNL) of the input–output characteristic of the converter. Increasing transistor size minimizes this effect, but this increases the chip area, thus limiting the maximum data resolutions in practice to only 7–8 bits.

The other technique that can be used to solve this problem has been described by Długosz, Gaudet, and Iniewski [29]. In this case, DAC has been realized as a cascade connection of two multistage current mirrors, where transistors do not need to be binary weighted. As a result, a smaller spread between transistor sizes and smaller chip area can be achieved.

In the classic single-stage binary-weighted approach, where the converter has the resolution of $n$ bits, the gain $k_x$ of the $x^{\text{th}}$ branch in DAC is equal to $2^{x-1}$. The DAC output reference current $I_{\text{ref}}$ is described as

$$I_{\text{ref}} = \sum_{x=1}^{n} I_{\text{ref}_x}, \text{ where } I_{\text{ref}_x} = k_x I_{\text{tr}} = 2^{x-1} I_{\text{tr}} \tag{11.4}$$

In the approach shown in Figure 11.14 the $I_{\text{tr}}$ current is copied $n$ times in the first DAC stage, creating $I_{\text{trx}}$ currents, which are then gained in the second stage, creating $I_{\text{refx}}$ currents. Particular reference currents are in this case given as

$$I_{\text{ref}_x} = k_{x1} k_{x2} I_{\text{tr}} \Rightarrow k_{x1} k_{x2} = 2^{x-1} \tag{11.5}$$

where $k_{x1}$ and $k_{x2}$ are gains of particular branches. A proper selection of coefficients $k_{x1}$ and $k_{x2}$ in each DAC enables significant minimization of the spread between transistor sizes that allows for increasing the size of all transistors. This technique is similar to that described by Abdelhalim, MacEachern, and Mahmoud [40] for a charge-redistribution voltage-mode SAR ADC, presented in the previous section. This approach has several advantages. It minimizes the mismatch effect, improves linearity of DAC, and allows for higher data resolutions. To obtain, for example, the resolution of 10 bits in a single-stage approach, the spread between transistor widths must be equal to 512. In the second approach, when gains of particular branches are properly selected, the maximum spread between transistor widths is only 32. Example gains of particular branches in both DAC stages can be selected as follows:

$$k_{x1} = \{1, 1, 1, 1, 1, 2, 4, 8, 16, 16\} \text{ and } k_{x2} = \{1, 2, 4, 8, 16, 16, 16, 16, 16, 32\} \tag{11.6}$$

Assuming that the width of the smallest transistor in DAC is considered to be a unity width (UW), the sum of all transistor widths for parameters given in Equation (11.6) is equal to 178·UW, in comparison to 1023·UW in the previous approach.

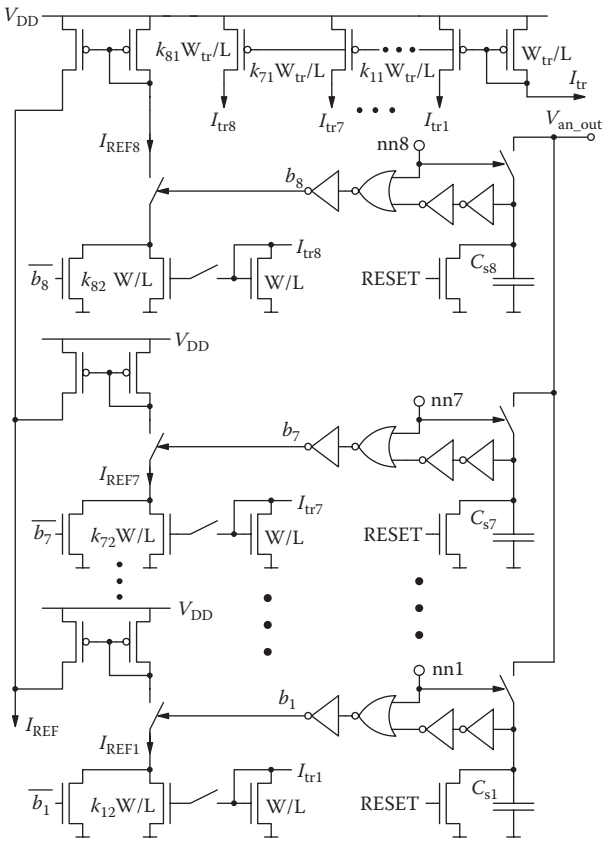


**FIGURE 11.14** Two-stage DAC with a controlling digital circuitry. (From Długosz, Gaudet, and Iniewski [29]. © 2007 by IEEE. With permission.)

This allows for increasing the value of UW and for minimizing the mismatch error. In this approach, each DAC stage introduces its own mismatch error. Assuming that the value of UW in both approaches is equal, the resultant error in the second approach will be larger by 5–10% than in the first one. On the other hand, increasing the value of UW 5.75 times (i.e., 1024/178), which is possible due to lower spread, lowers this error by up to 80%.

One of the disadvantages of the second approach is the increased number of branches in both DAC stages, resulting in slightly increased total current. The additional current is very small. For the example gains given in Equation (11.6), this is maximum $51 \cdot I_{tr}$, which is only ca. 5% of the maximal value of the reference current $I_{ref}$.

## 11.8 INTERLEAVED SAR OPERATION

A serious limitation of classic SAR ADCs is a relatively low data-conversion rate, which is equal to $f_S/n$. To overcome this problem, the interleaved SAR ADCs have

been introduced and are gaining popularity in recent years, especially in applications where a high data rate is required, e.g., in Ultra-Wideband (UWB) systems.

The general scheme of the interleaved converter is shown in Figure 11.15. This circuit consists of an analog demultiplexer at the input, a digital multiplexer at the output, and several equal channels working in parallel, where each of them contains a single classic SAR converter. A high-rate input analog data stream is directed to particular channels using the input demultiplexer, which is akin to a rotating switch, and is controlled by a central clock generator. In this way, each channel gets only a fraction of the input data and therefore may be sampled with reduced sampling frequency. Particular channels start conversion in different phases of the central clock generator and finish it also in different time moments. The results are combined into one output digital data stream using another rotating switch (multiplexer).

Particular channels operate at reduced frequencies, and therefore the interleaved approach puts lower demands on particular building blocks such as comparators and DAC, thus simplifying the design process for these blocks. On the other hand, an additional central control block is required to synchronize all channels in time, which makes the interleaved structure much more complex than the classic SAR converter. Interleaved converters occupy the chip area that is at least $n$ times bigger than in the case of a single converter.

Interleaved SAR converters, in comparison to flash converters, have several interesting features. One of them is high flexibility, meaning that their power dissipation and resolution may be easily controlled and matched to temporary conditions and system requirements. This is possible, as an SAR algorithm can be stopped at any time, and particular imaging channels may be turned off, when the input data rate is smaller.

In recent years, several interesting interleaved SAR converters have been reported, mostly designed using the voltage-mode charge-redistribution approach for UWB applications, where maximum resolution of 5 or 6 bits is sufficient, but where power dissipation is a critical criterion. These converters operate with very high sampling

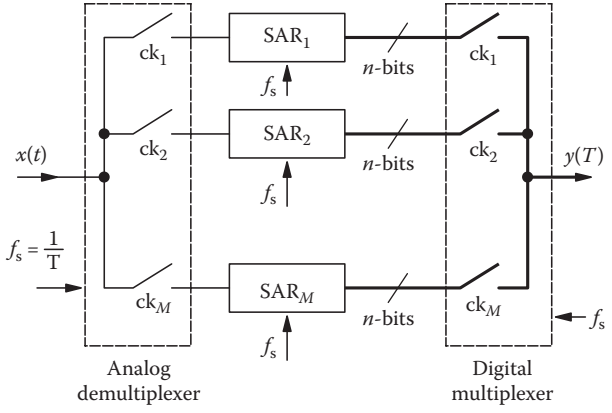


**FIGURE 11.15** The general idea of SAR interleaved ADC.

frequencies, between 500 MHz and 1.2 GHz, which so far were reserved rather for flash converters, achieving much lower power dissipation.

The relatively low resolution is mostly imposed by a capacitor array. Increasing the resolution by each additional bit means, in practice, almost doubling the chip area and power dissipation. The other reason for the low resolution is the comparator's offset. This problem can be solved by raising the input voltage swing, but this also raises the power dissipation of DAC.

Optimization techniques that usually are used in interleaved SAR converters to achieve better parameters are similar to those used in the single SAR converters we described earlier. Optimization of the capacitor array in DAC is one of these techniques. In general, the effective converter's resolution depends mostly on the linearity of the DAC, which depends on matching between capacitors. A typical method that relies on increasing the unity capacitor in DAC limits the maximum sampling frequency. This effect can be compensated by larger switches with lower on-resistance used in DAC, but this also enlarges the charge-injection effect. In the solution presented by Dondi et al. [45], this problem has been solved by using a boosting charge pump, which raises a gate-to-source voltage in switches, thus decreasing the on-resistance. This technique allows for the use of transistors with smaller widths and a reduction of the charge-injection effect. As a result, a sampling frequency up to 1.2 GHz is possible at the cost of 16 mW of power dissipation.

The other way to increase the conversion data rate is to introduce various self-timing techniques. In general, SAR converters do not require a very clean clock generator. The only task of the clock circuit is to start particular algorithm steps after the previous steps are completed. In this situation, time allocated for each step must be sufficient to settle the comparator's output. SAR converters typically are controlled by synchronous clocks, where the sampling frequency is adjusted to the worst-case scenario, i.e., when both comparator inputs have similar values and the resolving time is long. Such a situation might occur, for example, during the calculation of LSB. This approach is a source of time redundancy in other successive algorithm steps, which inherently limits the data-conversion rate. For example, one of these self-timing techniques has been used in the converter reported by Ginsburg and Chandrakasan [46]. In SAR conversion schemes, the comparative results from one step are used to prepare a new reference signal for the next step. A disadvantage of SAR architecture is that preparation of this new reference signal requires some additional feedback time. This time must be minimized to allocate as much time as possible to settle the analog signals in the capacitor array and preamplifier stages in the comparator. The self-timing technique described by Ginsburg and Chandrakasan [46] relies on minimizing this time. In this case, after the comparator resolves a value, the output latch triggers the next algorithm stage. In this situation, the remainder of the time initially allocated for the previous step may be allocated to the next step. This mechanism enables the extension of the settling time by about 20%.

The other self-timing technique has been reported by Chen and Brodersen [48], where an asynchronous clock generator was used to control a 6-bit interleaved SAR

converter. The presented technique allocates only as much time to each algorithm step as required to settle the comparator's output. When both comparator inputs differ significantly, then the comparator settles very quickly, and the next algorithm step can start immediately. This concept requires a special dynamic comparator that can generate a data-ready signal when comparison is completed. The comparator used in this converter has two complementary outputs, which during the reset phase are connected to the positive supply voltage, generating logical values 11. During resolving time, one of these outputs becomes 0. The data-ready signal is generated by an additional logic circuit, which distinguishes a 01 or 10 state from the previous 11 state. This technique is very effective, resulting in the best parameters between the converters described in this section. The converter dissipates 5.3 mW at a sampling frequency of 600 MHz.

A new interleaved 6-bit ADC suitable for high sampling frequencies above 1 GS/s and moderate power dissipation has recently been proposed by Cao, Yan, and Li [57]. In this converter, shown in Figure 11.16, two equal structures are interleaved in time and clocked with the sampling frequency of 1.25 GS/s each. This is a hybrid structure that involves both the flash architecture and the SAR algorithm. The top conversion scheme is the SAR one, while at each conversion stage a 2-bit flash converter is used. As a result, to calculate 6 bits, only 3 conversion steps are required. This converter is a compromise solution between the SAR and the flash structures. Instead of using 63 comparators, as would be the case in a 6-bit flash converter, in this case, the number of converters has been reduced to only 6, i.e., 3 for each channel. The power dissipation at the level of 32 mW is in this case higher than in previously described SAR converters, but it is still five to six times smaller than in

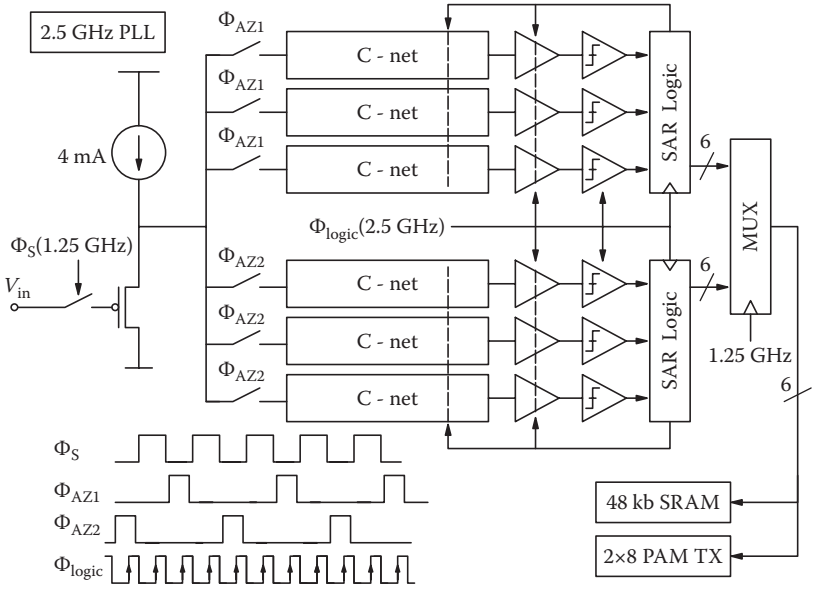


**FIGURE 11.16** Hybrid flash-SAR high-speed ADC. (From Cao, Yan, and Li [57]. © 2009 by IEEE. With permission.)

classic flash structures operating with the same frequencies [9]. The disadvantage here is the increased number of capacitors. However, a careful design of the capacitor array (C-net) allowed reducing the value of the UC to only 5 fF, which condensed the overall chip area to a relatively small 0.09 $mm^2$.

## 11.9 CURRENT-MODE INTERLEAVED SAR ADC

All interleaved converters described in the previous section have been designed for very high sampling frequencies in order to compete with flash architectures. Comparing these converters with flash counterparts designed for the same sampling frequency range [6, 8–10], we can see that the power dissipation in the interleaved SAR converters is about one order of magnitude smaller, while the chip area in both approaches is comparable. In most medical-imaging applications, a higher circuit complexity that offers lower power dissipation is fully justified.

The interesting question is whether there is any sense in using the interleaved SAR approach in the case of sampling frequencies, which can be easily attained by single SAR converters that feature a simpler structure and lower chip area. The answer in some cases is positive. When looking, for example, at the current-mode converter described in Section 11.4 and at the results shown in Figure 11.13, the conclusion is as follows. When higher sampling frequencies are required (e.g., 80 MHz) and when the chip area is not a critical parameter, then an interleaved SAR structure with eight channels working in parallel is a more efficient solution. In this case, the interleaved converter operating at 1-V supply consumes 10 pJ/bit at the sampling frequency of 80 MHz, while a single SAR converter operating at 1.8 V consumes a similar energy of about 9 pJ/bit, but for a smaller sampling frequency of 25 MHz.

An example current-mode interleaved SAR converter has been reported by Dlugosz and Iniewski [32]. This converter consists of eight parallel channels, each containing a single SAR block described in Section 11.4. This converter has been designed for applications where the input data rate can vary over a wide range, and where power dissipation is a main criterion. The central control-logic block used in this circuit puts those sections that are temporarily not used into the power-down mode. In this case, the circuit consumes only a small fraction of the energy it would otherwise use. In this ADC converter, particular sections wake up only when they receive the analog data for conversion, and are turned off immediately after completing the conversion task. This is illustrated in Figures 11.17 and 11.18. Power dissipation starts increasing when the first ADC section wakes up. Maximum current is reached when all eight sections are turned on and then decreases when the subsequent sections complete their conversion tasks. This converter implemented in TSMC 0.18-μm CMOS technology occupies a 0.1-$mm^2$ area and, at the sampling frequency of 1 MHz, dissipates 4 μW of power from a 0.65-V power supply. In standby mode, when all channels are off, the average power dissipation is 130 nW, consumed mostly by a central logic block.

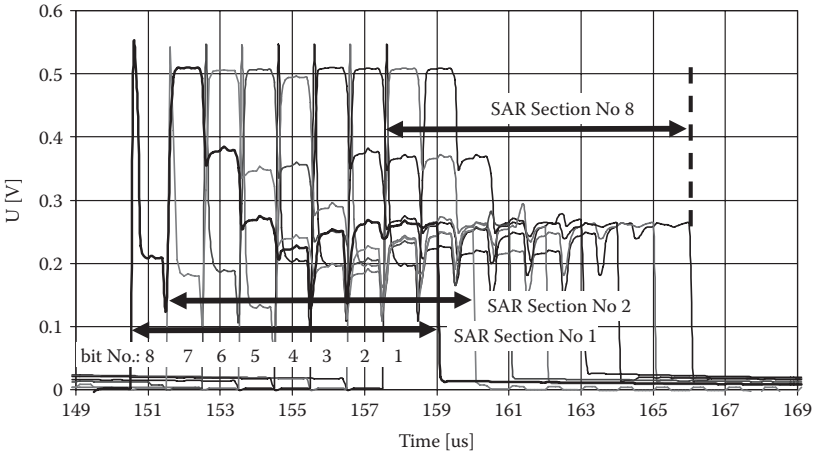


**FIGURE 11.17** Voltage waveforms at the comparator inputs, illustrating the interleaving action of eight SAR sections sequentially turning on and off. (From Dlugosz and Iniewski [32]. © 2007 by Hindavi Publishing. With permission.)

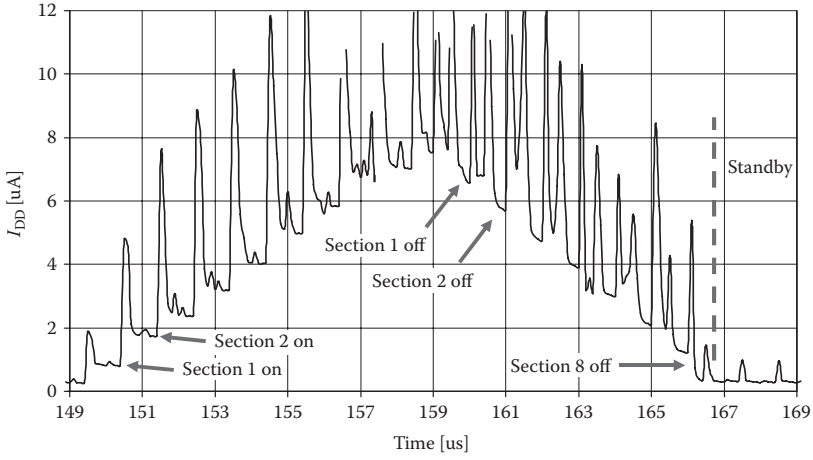


**FIGURE 11.18** Total current flowing in the converter during particular conversion steps and during the standby mode. (From Dlugosz and Iniewski [32]. © 2007 by Hindavi Publishing. With permission.)

## 11.10 CONCLUSIONS

X-ray medical-imaging sensors integrated with traditional CMOS circuitry are poised to enable a new era of digital imaging where images gathered using various imaging techniques will be processed, stored, and transmitted using well-known digital media. To achieve cost effectiveness of these techniques, a significant research effort is required both in imaging sensors and in the accompanying CMOS circuits. One

of the critical areas that requires further innovation is analog-to-digital conversion. In this chapter, we have reviewed different ADC design architectures and suggested that successive approximation (SAR) is the most power-efficient design technique.

A larger selection of SAR-based stand-alone commercial products is expected in the future, which will enable more power-efficient and integrated imaging systems. On-chip ADC integration with analog front-end circuitry that interfaces directly to X-ray sensors is also possible. However, common problems with noise cross talk, circuit thermal and flicker noise, manufacturing variations, and mismatch and low-voltage signal processing will have to be addressed in CMOS-chip implementations.

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