NEW ARCHITECTURE OF PROGRAMMABLE SC FIR FILTER WITH CIRCULAR MEMORY

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ABSTRACT: The paper concerns new finite impulse response filters (FIR) realized in the switched capacitor (SC) technique. Filters of this new type to a certain degree are based on the architecture of rotator filters. The new structure, however, has been modified to such an extent (the rotator switch has been eliminated) that it cannot be even called rotator filter of a new type. It was necessary to coin a new name – programmable circular memory filter – which adequately describes the new structure. The previous filter was designed by the author of this paper in CMOS 0.35μm technology. The present paper compares the new structure with the old one and points to both advantages and disadvantages of the new one. The advantages are numerous – with only few disadvantages. In the new filter the integrated circuit area has been reduced almost by 40% and the number of controlling clock signals by 50% and, as various parasitic capacities present in the rotator switch were eliminated, the precision of the structure has been greatly increased.

INTRODUCTION

This paper is devoted to the design and optimization of the finite impulse response (FIR) filters realized in the switched capacitor (SC) technique.
A generic block diagram for an FIR filter is shown in Figure 1. The filter of N order contains a delay line, which stores N signal samples. The samples of the input signal passing through this line are multiplied by N+1 filter coefficients h_i and then summed to produce a sample of the output signal. This general principle can be realized using various architectures. The differences among them lie in the construction of particular building blocks with the delay line at the top. Signal samples in SC FIR filters are represented as voltages on capacitors. In some filter structures the samples are copied many times between subsequent delay elements, which leads to relatively serious errors, and, in consequence, to inaccuracy visible especially in the stopband for filters of higher orders [6, 7, 8]. This situation is to be found in the "even-odd", Fisher and Gillingham delay line structures [4, 7]. There are also other SC FIR filter architectures, in which delay line is constructed in a different way. In filters of these types circular analog memory is used, and samples are not copied between memory cells. In rotator filter structures particular memory cells store only one signal sample [4, 9]. Instead, in the multi-C structure the memory cells store more than one signal sample in parallel [4].
This paper presents the new architecture of SC FIR filter. The new filter adopts some blocks from SC FIR rotator structure previously realized in the CMOS 0.35 μm technology [9]. The new filter presented in this paper is an improved version of the rotator filter. However, as the changes introduced into the structure are of substantial nature and comprise also the block which gave the name to the prototype – rotator switch – the new filter has been called circular memory SC FIR filter structure. This name in a considerable degree corresponds to the basics of the new structure. The rotator switch of the old type influenced the configuration of the analog signals processed by filter. The rotator switch connected analog cells outputs to various capacitors in the summer circuit. Filter coefficients did not change during the work of the filter. In the new structure the rotator switch has been removed and there has been introduced a permanent connection between the cells and capacitors. Also, the application of the circular memory introduced a rotation change of coefficient values during the work of the structure.

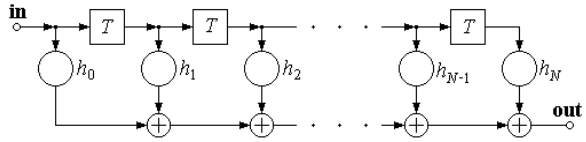

Fig 1. Block diagram of a finite impulse response (FIR) filter with three layers: delay line (delay elements T), filter coefficients (h_i), and the summer circuit

In the following part of this paper the previous version of the SC FIR rotator filter structure is shortly presented and evaluated. This chapter also discusses various disadvantages of this kind of filter.
In the third part of the paper the new SC FIR circular memory filter is presented with such aspects as the general basics with potential application of the filter, the realization of new clock generator, the realization of the circular memory block. The conclusions of the discussion are presented at the end of the paper.

SC FIR ROTATOR ARCHITECTURE – PREVIOUS FILTER TYPE

The rotator filter is an interesting solution and this in many respects. The principle of its working is the

following: the input signal samples are copied into subsequent elements of the analog – circular memory of the sample & hold type, and are not being repeatedly rewritten between the memory elements - as it is the case in structures with delay lines. S&H elements make it possible to repeatedly read the signal samples without these being deleted - as it was the case with Gillingham delay elements and "even-odd". The rotator switch controlled by multi-phase clock system causes switching over of the circuit in such a way that the capacitor inputs in filter coefficients read samples from different delay elements, thus realizing the delay effect of subsequent signal samples. The result is that the signal samples are rewritten in the structure several times only. The number of the rewriting operations does not depend on the length of the filter. This solution allows to avoid errors accompanying the rewriting of the samples, which happened in previously realized projects. The circuit is controlled by a complex clock system in which the real number of various signals is four times greater than the length of the filter and can be expressed by the following equation:

$L_{\mathrm{PHOLD}} = 4\,(N+1) + 4$, where N – is the filter order (1)

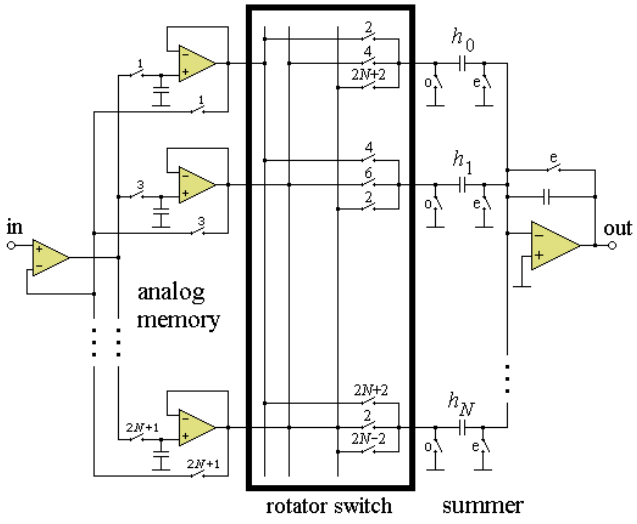

Fig 2. Electrical diagram of SC FIR rotator structure

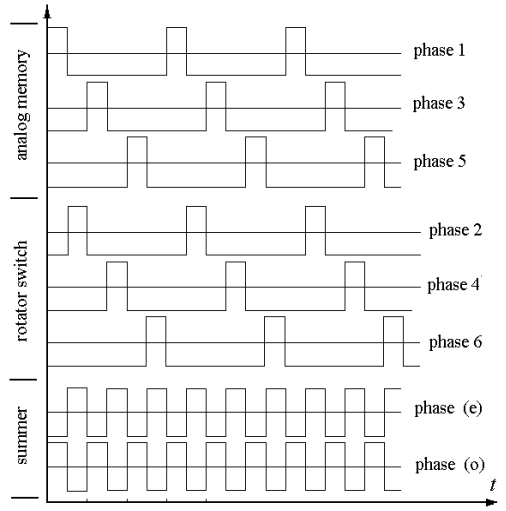

Fig 3. Illustrative clock diagram for the filter of order N = 2

Scheme of the SC FIR rotator filter is shown in Figure 2. Example time diagram of clock signals for $N = 2$ is shown in Figure 3. Each of these signal must have its negated counterpart – it is because the keys realized as transmission gates are controlled with complementary clock signals. The rotator filter (for the order $N = 15$) has been implemented in CMOS CSX 0.35µm technology in EUROPRACTICE (Figure 4). The design is described in [9]. The block scheme of a 66-phase clock system controlling the realized rotator filter is shown in Figure 5. The clock generator is described in detail in [10]. This clock is based on the self-correcting counter which contains 16 D-flip flops. With two external signals **clk**, **clk1** and additional elements one can obtain 66 controlling signals.

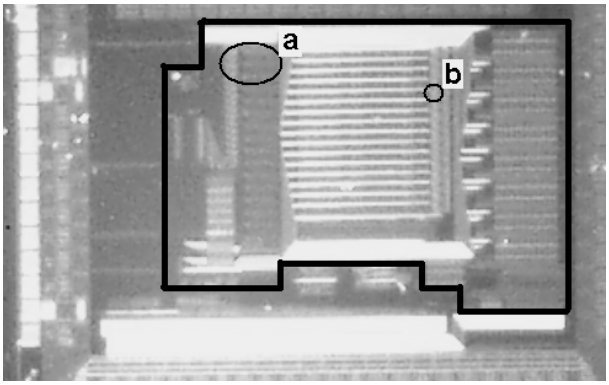

Fig 4. SC FIR rotator filter designed in the CMOS CSX 0.35 µm technology; (a) – a part of the rotator switch zoomed in Fig. 6, (b) – configuration block of the filter coefficient zoomed in Fig. 9

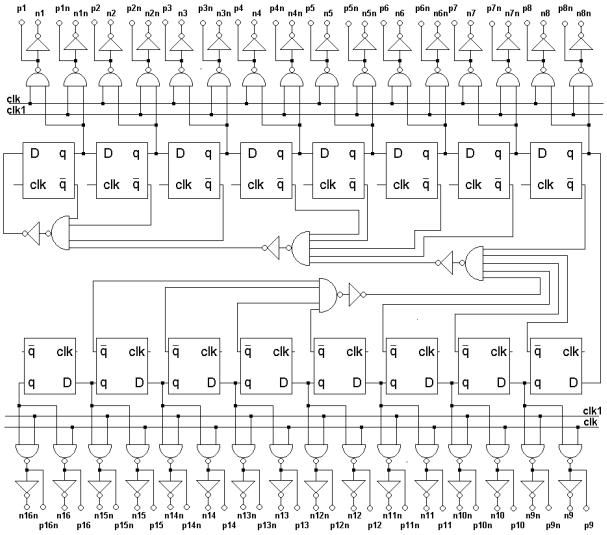

Fig. 5. Clock generator implemented together with previous SC FIR rotator filter in the CMOS 0.35µm technology [10]

Disadvantages of the SC FIR rotator filter

The main disadvantage of the rotator filter FIR with the rotator switch is the necessity of using this key. This problem is caused by that in the rotation switch (fragment of such a key is shown in Figure 6) outputs of all analog memory cells (delay elements) must cross

each of these outputs in CMOS hardware implementation. Between the paths of these outputs there exist parasitic capacities, which influence the precision of the filter. The rotator filter causes the switching of the configuration of the structure in the analog part, so it directly influences the processed signal. The problem is that signals coming from particular outputs flow along the lines of different lengths. The result is that respective samples are being sent in different conditions (different propagation times, different values of parasitic capacities). Signal samples have – from the point of view of the filter – values which, in a large measure, are accidental. That is why each sample stored in coefficients is burdened with a certain accidental error. Quite another problem is that that the rotation switch occupies a relatively big area – c. 0.2 mm^2 for the filter length 16 (the filter length determines the number of coefficients and in the case of FIR filters is greater by 1 than the order N of the filter).

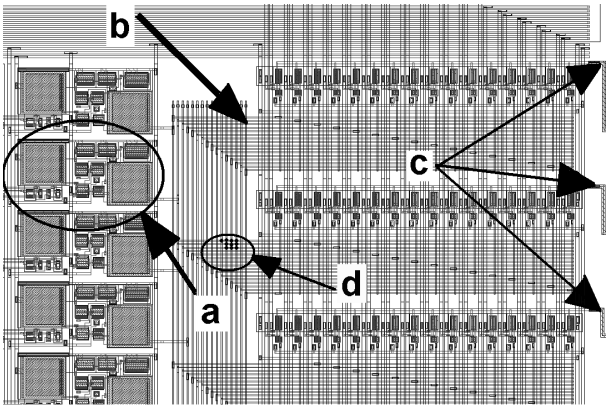

Fig. 6. Layout of the rotator switch with (a) analog memory cells (s&h delay elements),(b) rotator switch inputs, (c) rotator switch outputs (d) parasitic capacitors between analog memory outputs

Another disadvantage of the rotator switch is that to control it there are required additional clock signals. The number of these signals amounts to almost a half of all signals in the filter. In the realized project of the filter the number of the clock signals in the rotation switch is 32.

SC FIR CIRCULAR MEMORY FILTER

Applications of the new filters

It must be said that the new filter can work only if the coefficients are programmable. In certain situations it is a disadvantage of the structure because it is not always necessary to use the programmable filter (e.g. when the characteristics of the filter are established [6, 7]). In a programmable circuit each coefficient must have the same structure and capacitor capacity, because it is difficult to foresee what filter characteristics will be finally programmed. In this case there exists such a excess that some of the capacitor segments remain inactive at the given moment. This solution requires an area bigger than it is necessary in the case of not programmable structure. However, this is not a very serious problem. Programmable filters are more and more often examined because of various new applications which are opening for them – for example channel filters, which may be switched to different standards, are used in WCDMA telecommunication [1, 2]. So, the described problem is the only disadvantage of the filter when compared to the previous rotator filter solution.

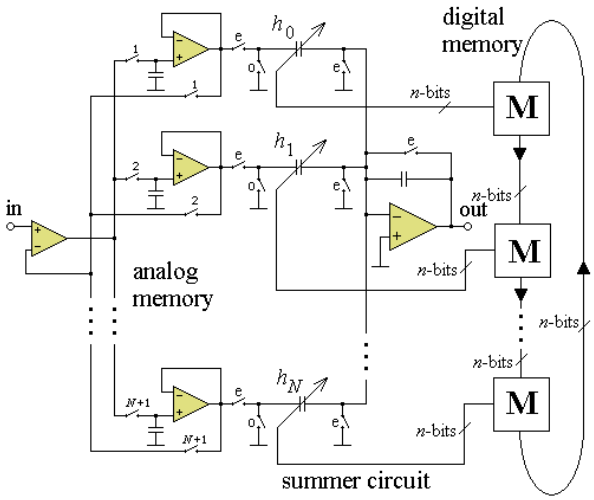

Fig 7.Electrical diagram of SC FIR circular memory filter

The basis of the structure of new filters

The structure of the new filter is mostly based on SC FIR rotator structure. The electrical scheme of the new filter is shown in Figure 7. In this new structure some blocks have been solved in an entirely different way than it was in the case of the rotator filter. The result is a considerable simplification of the whole circuit structure. The first and simultaneously the most important innovation consists in removing of the uncomfortable rotator switch. In the new filter each delay element corresponds to only one capacitor. There is no switching over of delay element outputs to various coefficients. However, in order to cause a similar effect as in the rotator switch, which in turn will effect a similar reaction of the circuit, rotation was relocated to another place. Previously filter coefficients had definite values which did not change when the circuit was working. Now coefficient values change when the circuit is working and these changes take place in a cyclical way – from one sample to the other. Coefficient values are being rewritten between capacitors. The advantage of this solution is that the switching over takes place on the side of the digital memory, which stores values of filter coefficients – i.e. far from signal lines. The change of configuration takes place during the so called dead periods, i.e. after coefficient capacitors have been discharged through the output op amp. The change of the configuration itself is a quick process, in practice it is not perceptible for the system. The eliminating of the rotator switch leads automatically to the elimination of over 300 critical parasitic capacities (for the filter of $N = 15$ order). The number of parasitic capacities in the rotator switch

increases with square of the filter length and is expressed by the following equation:

$$L_{PCR} = (N + 1)^2 \qquad (2)$$

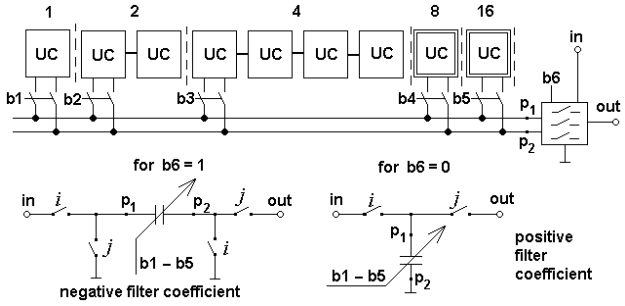

Fig 8. Programmable coefficient capacitor: bits b1-b5 connect sections of 1, 2, 4, 8, 16 of unit capacitors (UC's) to the line (totally 31 UC's can be connected), an additional bit b6 changes configuration (negative or positive sign of the filter coefficient)

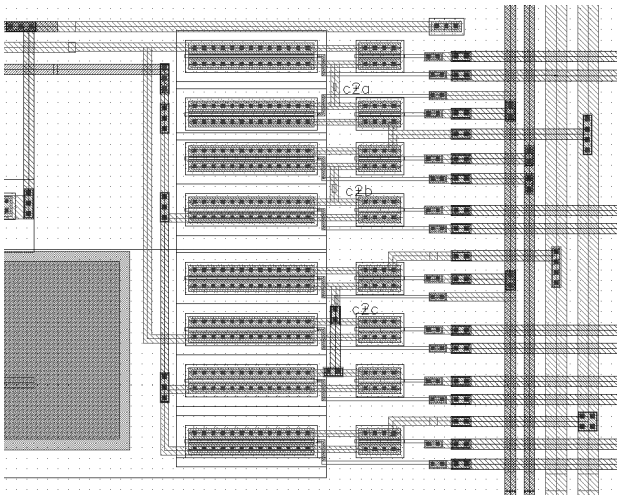

Fig.9. Layout of the configuration circuit controlled by bit b6.

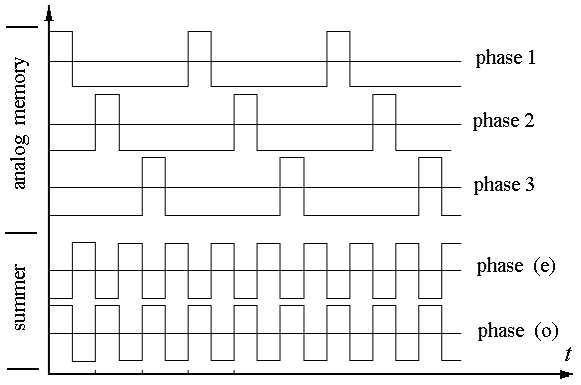

Fig 10. Illustrative clock diagram for the filter of order N = 2

Filter coefficients are programmed with *n*-bit words (for the implemented design of filter $n = 6$). The scheme of a block of programmable capacitors is shown in Figure 8. The absolute value of the capacitor capacity is programmed with 5 bits. The 6th bit changes the sign of the coefficient through the change of the structure configuration. The layout of the structure which changes configuration of the filter coefficient is shown in Figure 9. The way in which capacitors in the circular memory filter are programmed is the same as in the case of the rotator structure.

Clock generator in new filters

The removal of the rotator switch results in substantial simplification of the clock system. The rotator switch requires additional clock phases, the number which is $2(N+1)$. In filters of the new type the number of the clock signals was reduced approximately by half and can be expressed by the following equation:

$$L_{PHNEW} = 2(N+1)+4 \qquad (3)$$

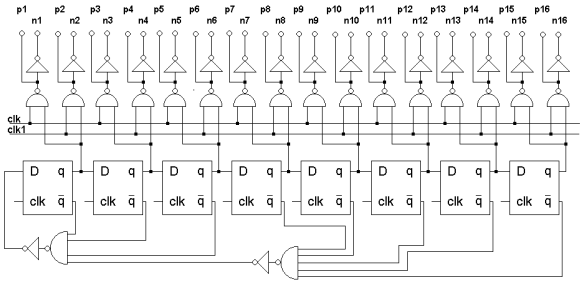

Fig. 11. Clock generator for SC FIR circular memory filter of order N=15 (first variant)

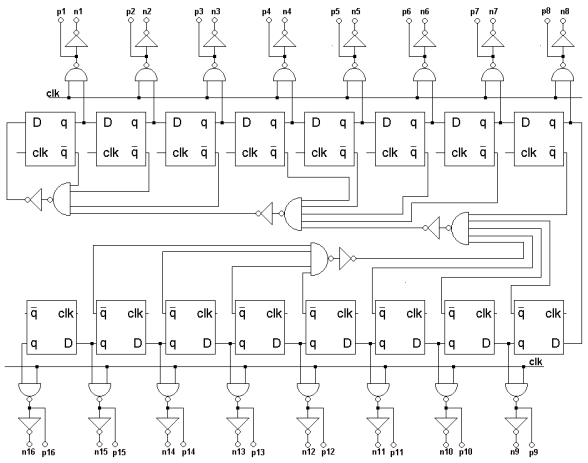

Fig. 12. Clock generator for SC FIR circular memory filter of order N=15 (second variant)

An example time diagram of the clock signals for filter of order $N = 2$ is presented in Figure 10. The clock signals are doubled for the same reason as previously. Equations (1) and (3) take into account all clock signals. Clock generators for filters of the new type can be realized in various ways. In the first approach (see Figure 11) the number of D-flip flops in the counter is simply reduced. Signals **clk** and **clk1** are still necessary, but frequency with which these impulses appear must be smaller by a half than frequency of the clock signals (e) and those (o) used in the summer circuit. It is a disadvantage, as in the rotator filter **clk** and **clk1** signals were used directly – as signals (e) and (o). This problem can be solved quite simply with an additional looped D-flip flop controlled with signal (o), of which output **q** now will be **clk** signal. In this case the reduction of the area will be slightly less than 50 %. In the second

approach shown in Figure 12 the number of D-flip flops in the ring counter will remain unchanged. However such additional elements as gates will be reduced by a half. In this case only one controlling signal **clk** is necessary – it is also used as signal (o). Apart from that, an independent signal (e) is necessary as well. The reduction of the chip area amounts to c. 25%, but this structure has a less complex construction. Also, there are no problems with synchronization of signals (e), (o) with those controlling analog memory. In the first case synchronization remains a problem to be solved.
Considering various aspects, the first approach seems to be a better solution after the optimization. The reduction of the number of clock phases by half not only leads to the reduction of the clock system area but – which is even more important – to the reduction of the area of the clock signal lines, as well. In this case the reduction of the chip area is even greater because the number of paths is reduced by half and, in addition to this, the clock signals are being sent to one block only – to the input analog memory; but before that these signals had to be brought to the rotator filter.

Digital memory in filters of the new type

The new filter has a more complex digital memory block which stores capacitor values. The memory can be realized in more ways than one. One of them consists in modifying of the existing solution through the implementation of the mechanism, which enables cyclical rewriting of data between adjacent memory segments. This mechanism will remain inactive during the period of preliminary filter programming and be activated later. In this case it is necessary to add keys connecting outputs of one memory segments with inputs of the subsequent segments – closed after the filter has been programmed. The number of these keys must be equal to the number of the memory cells. The transistors in these keys can be very small and, consequently, will influence the circuit area in a very limited degree. This solution is possible with the use of an address decoder and address lines – as it was in the implemented rotator filter [9]. The advantage of that structure was that it was possible to quickly change the value of particular coefficients. This, however, is of no use in the new filter, in which the values of particular coefficients, because of continuous rewriting, can be in various memory segments which makes it difficult to locate them.
An entirely different solution can be applied in the new filter. The data inputs will be permanently connected to the first memory segment. When the data have been stored in this segment, in the following cycle they will be copied into the next segment, and simultaneously their place in the first segment will be taken by a new data. In subsequent cycles data will be rewritten into next segments. In this way, during several cycles of the clock, the whole memory capacity will be filled with data. As two-stage memory has been used in the structure, all the data are being rewritten in parallel. During the preliminary programming process the connection between the last segment and the first one, which normally closes the ring, must be broken, so that the accidental values – present in the memory after the structure has been switched on – are not copied into the earlier programmed segments. After all the data have been copied, the ring is closed, and in subsequent clock cycles that data rotate between the segments. Advantages of this solution are numerous, indeed. One of these is that it is possible to ignore the bus lines and address decoder which leads to the reduction of the area and simplification of the structure. Moreover, it is not necessary to use connecting keys between memory segments nor any additional signals controlling these keys.

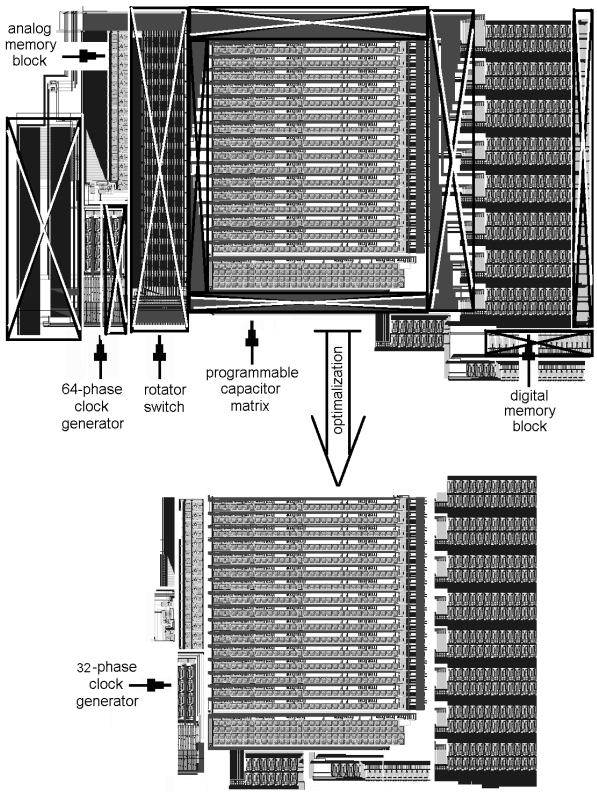

Fig. 13. Top - a layout of the rotator filter (marked are these blocks that can be omitted in the new filter). Bottom – blocks which must remain in the new filter. The chip are has been reduced by more than 40 % and can be further optimized – mostly by the application of memory cells of a different type.

SUMMARY

This paper presents a new type of analog FIR SC filter with circular memory. This structure is a modification of SC FIR rotator filter structure which was designed in CMOS CSX 0.35μm technology. As the changes are of substantial nature – e.g. removal of the rotator switch – the new structure got a new name which reflects its specificity – the circular memory filter.
The filter proposed in this paper has not been realized yet. However, as it mainly consists of the blocks of the previous structure, it is possible to foresee its properties. The new structure has a lot of advantages – they are shortly summarized in Table 1. The most important of them are: the substantial reduction of the chip area by c. 40%, simplification of the clock signal generator and the expected increase of filter precision. This last thing

is the result of the simplification of the structure – as far as the analog signals are concerned, which, in turn, reduces substantially the number of parasitic capacities – these, because of their position in the structure, can influence the processed signals in a considerable degree. The structure may be used in various applications – mostly in telecommunication. One of them is the channel baseband filter for the third-generation (3G) cellular phone systems such as WCDMA [1, 2]. This filter can also be used in many other adaptive signal processing tasks, such as industrial control systems, new generation hearing aids, etc.

TABLE 1. General comparison between two described filters

	SC FIR rotator filter	SC FIR circular memory filter
Filter order *N*	15	15
Number of clock Phases	66	36
Chip area	2.2 mm^2	1.3 mm^2
Power Consumption	8 mW	8 mW
Other parameters		Better accuracy Simpler structure

The chip area of the designed SC FIR rotator filter occupies c. 2.2 mm^2 (linear dimensions are equal to 2000 μm × 1100 μm). Preliminary calculations show that the filter of the new type will occupy only about 50-60 % of the chip area. Digital memory, which stores filter coefficient values, will be optimized. Its miniaturization will further reduce the chip area by c. 0.2 – 0.3 mm^2. The assumed task is to implement in one structure two such filters connected in cascades. This will make it possible to significantly increase selectivity of the structure. A similar solution was applied in the previous filter prototypes [6, 7].

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