Dr. Eng. Rafał Długosz

University of Sciences and Technology

Faculty of Telecommunications, Computer Sciences, and Electrical Engineering

Bydgoszcz, Poland

An application for processing a habilitation proceeding in the domain of technical sciences in the discipline electronics

Statement of research activity

Poznań, September 2015

Spis treści

1 Obtained titles and degrees

- 06/2004: PhD in Telecommunications – specialization Signal Processing. Faculty of Electrical Engineering, Poznań University of Technology. Thesis entitled: "Design and optimization of finite impulse response filters electronic integrated in the CMOS technology".
- 09/1996: Master of Science in the field of Control and Robotics, Faculty of Electrical Engineering, Poznań University of Technology. Thesis entitled: "Implementation of New Algorithms for Adaptive Control of Industrial Robots".

2 Employment history and research stays at other universities

- 07/2014 – now Delphi Automotive, R&D Active Safety Team Leader, Kraków, Polska
- 10/2010 – now Assistant Professor, University of Science and Technology, Faculty of Telecommunications, Computer Sciences, and Electrical Engineering, Bydgoszcz, Poland
- 10/2002 – now Senior Lecturer, College of Computer Science in Łodź, Department in Bydgoszcz, Poland
- 08/2010 – now Consultant – Senior Scientist (Analog Design Services), CMOS Emerging Technologies Research Inc. 1-1125 Kensal Pl., Coquitlam, BC, V3B 0G3, Canada
- 12/2012 – 02/2013 Scholarship in the Industrial Institute IHP (Innovations for High Performance Microelectronics – formerly the Institute für Halbleiterphysik), Frankfurt/Oder, Germany. The scholarship granted by DAAD (Deutscher Akademischer Austauschdienst) research foundation — Hardware realization of a low chip area (0.01 mm^2) 10-bits, current-mode, successive approximation register (SAR) analog-to-digital converter and a new digital, asynchronous circuit used to detect winning neurons in hardware Kohonen neural networks.
- 01/2009 – 12/2012 Swiss Federal Institute of Technology in Lausanne (EPFL), Institute of Microtechnology (IMT), Electronics and Signal Processing Laboratory (ESPLAB), Switzerland (01/2012 – 12/2012 Invited Professor, part-time position, three-months in total)
- 09/2006 – 12/2008 University of Neuchâtel (IMT ESPLAB), Switzerland – EU Marie Curie International Outgoing Fellowship (IOF) – 6^{th} Framework Program (09/2006 – 08/2008 seconded to the University of Alberta in Canada)
- 09/2005 – 08/2008 Postdoctoral fellow, Department of Electrical and Computer Engineering (ECE), University of Alberta, Edmonton, Canada (two postdoctoral scholarships). In 2012 a 1-month research stay at the University of Alberta as a Visiting Professor (hardware implementation of selected blocks for neural networks).
- 06/2006 Internship, Scanimetrics, Edmonton, Canada (`http://www.scanimetrics.com`)
- 10/2004 – 09/2010 Assistant Professor, Department of Computer Science and Management, Institute of Control and System Engineering (CSE), Poznań University of Technology (PUT), Poland (since 09/2005 scientific leave)
- 10/2001 – 09/2004 Research Assistant, CSE PUT, Poland
- 10/1996 – 09/2001 Research Assistant, Faculty of Electrical Engineering, Institute of Electronics and Telecommunications, (PUT), Poland
- 10/1999 – 03/2000 Industry institute IHP - Innovations for High Performance Microelectronics, Frankfurt/Oder, Germany

3 Overview of scientific achievements

Statistical summary of research achievements of the author is shown in Table 1. It includes publications, participation in research projects and scholarships. Full list of publications published after obtaining the PhD degree is in the following sections.

Tablica 1: An overview of scientific achievements

L.p.	List of achievements	Before PhD	After PhD	Total
1	Publications in jornals from the Journal Citation Reports (Philadelphia List)	1	15	16
2	Publication in other peer-reviewed journals (domestic or foreign)	0	19	19
3	Authorship chapters in monographs or academic textbooks in English	1	4	5
4	Publications in materials of international scientific conferences	24	75	99
5	Participation in research projects in Poland	4	1	5
6	Participation in the international research projects	2	5	7
7	Scholarships (domestic and foreign)	1	5	6

3.1 Impact factor and scores on the basis of ministerial lists A and B

Tables 2 and 3 present Impact Factor (IF) and the scores on the basis of current ministerial lists A and B (XII 2014) of all papers published after obtaining doctorate degree in journals and chapters in scientific monographs.
(*) At the time of the publication the journal was on the Philadelphia List.
The total number of scores for publications in scientific journals and as book chapters, on the basis of statements presented in Tables 2 and 3, equals 610.

3.2 Citations of the author's papers

Citations as well as the Hirsch index were checked on the basis of the Web of Science database. The results are shown in Figure 1.

The Web of Science database does not include the newest citations of some of the the author's papers. Supplemented list of citations is presented in Appendix A. It is also worth noting that most of the author's publications on the Philadelphia List appeared in the last six years. Citations which are reported in the database cover relatively short period of time.

3.3 Scientific Scholarships at Universities and Institutions in Poland and Abroad

After obtaining the PhD degree the author received three prestigious scholarships, under framework of which he spent more than five years abroad.

1. The first grant he received from the Foundation for Polish Science for a one year stay at the University of Alberta in Edmonton, Canada, where he cooperated with Prof. Krzysztof Iniewski and Prof. Witold Pedrycz. This co-operation is still continuing.

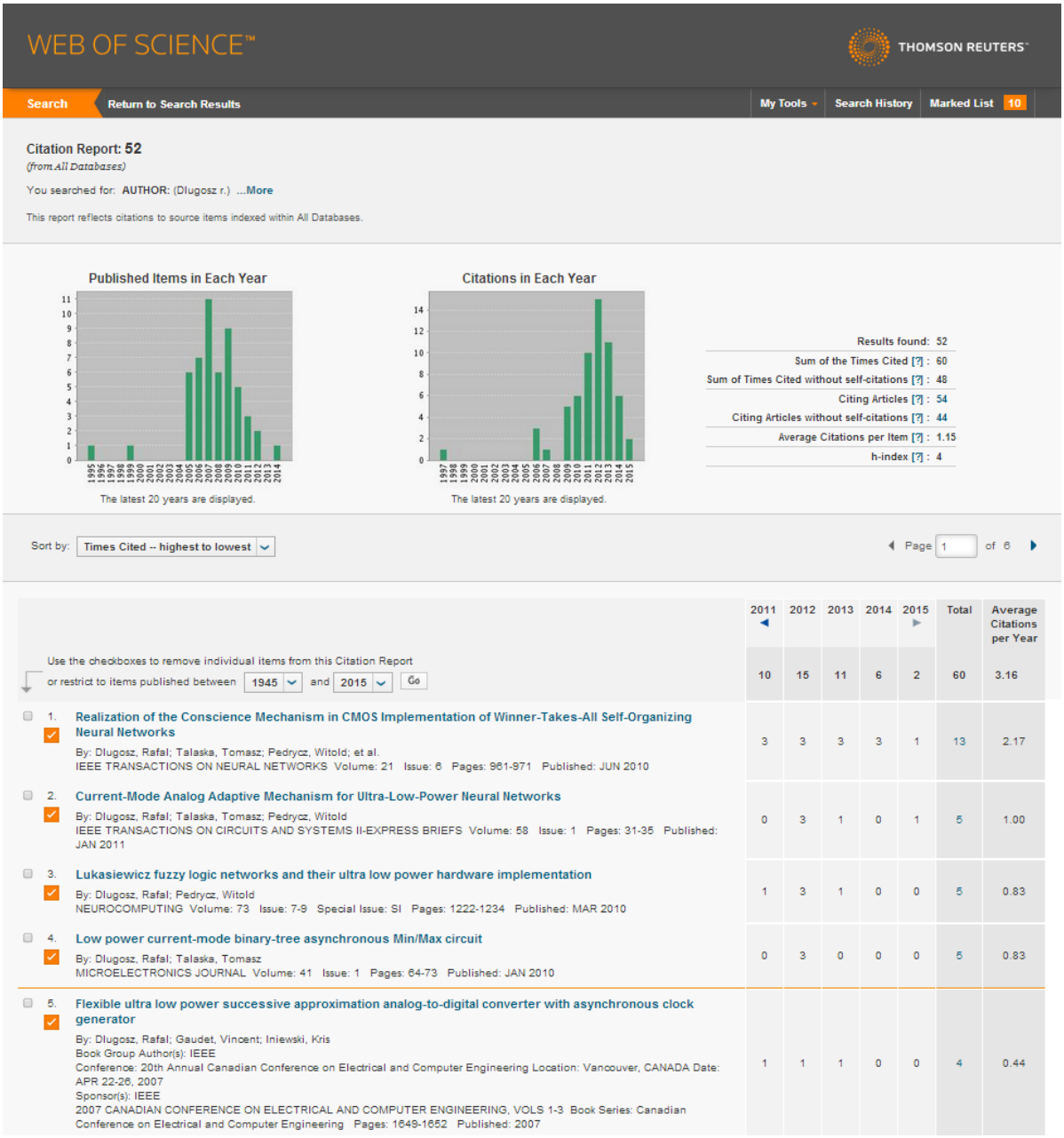
Tablica 2: Impact Factor and scores for papers in journals from the Philadelphia List (list A)

L.p.	Journal	IF (Scores)	No. of publications	Total IF (Scores)
1	IEEE Transactions on Neural Networks	4.370 (45)	3	13.110 (135)
2	Elsevier – Neural Networks	2.076 (30)	1	2.076 (30)
3	IEEE Transactions on Circuits and Systems (II: Express Briefs)	1.187 (25)	1	1.187 (25)
4	Elsevier – Microelectronics Journal	0.924 (20)	2	1.848 (40)
5	Elsevier – Microelectronics Reliability Journal	1.214 (20)	1	1.214 (20)
6	Elsevier – Neurocomputing	2.005 (30)	1	2.005 (30)
7	Elsevier – Applied Mathematics and Computation	1.672 (40)	2	3.344 (80)
8	Electronics Letters	1.068 (25)	1	1.068 (25)
9	Springer – Journal of Signal Processing Systems	0.564 (20)	1	0.564 (20)
10	Electrical Review (Przegląd Elektrotechniczny) (*)	0.244 (15)	2	0.488 (30)
11	Bulletin of the Polish Academy of Sciences-Technical Sciences	1.000 (30)	1	1.000 (30)
	Total		16	27.904 (465)

Tablica 3: Scores of other papers published in national and international journals (List B)

L.p.	Journal	Scores	Number of publications	Total Scores
1	Chapters in books (Springer and CRC Press)	7	4	28
2	International Journal of Electronics and Telecommunications	8	1	8
3	Elektronika : konstrukcje, technologie, zastosowania	6	6	36
4	Journal of Solid State Phenomena	10	5	50
5	Journal of the University of Science and Technology	4	2	8
6	Journal of Silesian University of Technology – Elektryka	4	1	4
7	Machine Graphics & Vision	7	1	7
8	Poznan University of Technology Academic Journ. of Electr. Eng.	4	1	4
9	Facta Universitatis, Series: Electronics and Energetics	0	1	0
	Total		22	145

2. The second three-years scholarship he received under the EU Marie Curie 6^{th} Framework Programme. As part of the scholarship he spent two years at the University of Alberta in Canada, and then one year in Switzerland, initially working at the University of Neuchâtel



Rysunek 1: The number of citations (48) and the Hirsch index ($h = 4$) on the basis of the Web of Science database

(UniNE) and then at the Ecole Polytechnique Fédérale de Lausanne (EPFL). In the meantime the Institute of Microtechnology has been moved from UniNE to EPFL. At the end of the two scholarships EPFL authorities extended the contract with the author by another year.

3. Cooperation with EPFL was continued after finishing the contract with this Institution. In 2012, the author received from the EPFLan invitation. As a result, he spent two months in Switzerland, working as Invited Professor. The cooperation with the University of Alberta is still continued, which is reflected in many co-authored publications with Prof. Witold Pedrycz. In 2012, the author spent one month at the University of Alberta in Canada working as Visiting Professor.

4. After coming back to Poland the author received from the Foundation for Polish Science a 1-year return grant for former beneficiaries of the Kolumb Program. The grant was realized at the University of Science and Technology in Bydgoszcz. During this period of time, in 2012, the author spent one month at the University of Alberta as Visiting Professor.
5. In 2012, the author received the scholarship from German DAAD (Deutsche Akademische Austauschdienst) Foundation. In between December 2012 and February 2013 he spent three months in the Industrial Institute Innovations for High Performance Microelectronics (IHP) in Frankfurt (Oder) / Germany.
6. In 2013 the author was beneficiary of the program "Knowledge for Business" organized by European Center for Financial Advisory in Poznań (six months in-between April and September 2013).

During his stays abroad the author actively participated in several research projects, collaborating with several industrial institutions in Canada and Switzerland (Colibrys, Scanimetrics, Redlen Technologies).

More details concerning described scholarships and realized projects are presented in section 5.2.

4 Indicated research achievement

Under the "Article 16, Paragraph 2 of the Act of 14 March 2003 on Academic Degrees and Title and Degrees and Title in the Field of the Art" the author indicates as his achievement the series of seventeen mono-thematic publications under the title:

**"Analog and Analog-to-Digital Reconfigurable
Low power Integrated Circuits
Working in Parallel and/or in the Asynchronous Fashion"**

4.1 List of publications concerning the indicated achievement

Personal percentage is given in parentheses at the end of each item. At the beginning of each item in square brackets are acronyms of particular papers added to facilitate orientation in Section 4.2.5. Some of the presented works are conference papers. In most cases they have been added since the author's participation in them equals 100 %. These papers have been next extended in journal papers or as book chapters.

Articles listed below are arranged largely by chronological order in which particular works were carried out. This is important as often the ideas proposed in some projects after modifications were used in the next ones.

1. [**MIXDES FIRSC**]R. Długosz, "New Architecture of Programmable SC FIR Filter with Circular Memory", *12th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Kraków, Poland, pp.153–158, (June 2005) **(100 %)**
2. [**SPR FIRSC**] R. Długosz, K. Iniewski, "Programmable Switched Capacitor Finite Impulse Response Filter with Circular Memory Implemented in CMOS 0.18μm Technology", *Journal of Signal Processing Systems* (formerly the *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology*), Springer New York, Vol. 56, No. 2-3, pp. 295–306, (September 2009), **(85 %)**
3. [**MIXDES GVM**] R. Długosz, "Analog, Continuous Time, Fully Parallel, Programmable Image Processor Based on Vector Gilbert Multiplier", *International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Ciechocinek, Poland, pp.231–236, (June 2007), **(100 %)**

4. [**SPR GVM**] R. Długosz, V. Gaudet, R. Wojtyna, "Gilbert-Multiplier-Based Parallel 1-D and 2-D Analog FIR Filters for Medical Diagnostics", Chapter 9 in *Computers in Medical Activities*, Book series: Advances in Intelligent and Soft Computing, ISSN: 1615-3871, ISBN: 978-3-642-04461-8, Vol. 65 / 2009, pp. 85-99, Springer-Verlag, Berlin / Heidelberg, (2009), **(75 %)**
5. [**BIODEV GVM**] R. Długosz, V. Gaudet, "An Asynchronous Programmable Parallel 2-D Image Filter CMOS IC Based on the Gilbert Multiplier", *International Conference on Biomedical Electronics and Devices* (BIODEVICES), Porto, Portugal, pp.46–51, (January 2009), **(90 %)**
6. [**VLSIDES ADC**] R. Długosz, K. Iniewski, "Flexible Architecture of Ultra-Low-Power Current-Mode Interleaved Successive Approximation Analog-To-Digital Converter for Wireless Sensor Networks", *VLSI Design Journal*, Hindavi Publishing, VLSI Design, Vol. 2007, Article ID 45269, 13 pages, DOI:10.1155/2007/45269, (2007), **(75 %)**
7. [**CRC ADC**] R. Długosz, K. Iniewski, "Analog-to-Digital Converters for Radiation Detection Electronics", Chapter 11 in *Electronics for Radiation Detection (Devices, Circuits, and Systems)*, CRC Press, 1st edition, ISBN-10: 1439816484, ISBN-13: 978-1439816486, (edited by: K. Iniewski), pp.285–312, (August 05, 2010), **(80 %)**
8. [**MIXDES ADC**] R. Długosz, G. Fischer, "Low Chip Area, Low Power Dissipation, Programmable, Current Mode, 10-bits, SAR ADC Implemented in the CMOS 130nm Technology", *International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, **accepted**, (June 2015), **(90 %)**
9. [**TNN CONS**] R. Długosz, T. Talaśka, W. Pedrycz, R. Wojtyna "Realization of the Conscience Mechanism in CMOS Implementation of Winner-Takes-All Self-Organizing Neural Networks", *IEEE Transactions on Neural Networks*, Vol. 21, Iss.6, pp.961–971, (June 2010), **(40 %)**
10. [**TCAS ADM**] R. Długosz, T. Talaśka, W. Pedrycz, "Current-Mode Analog Adaptive Mechanism for Ultra-Low Power Neural Networks", *IEEE Transactions on Circuits and Systems–II: Express Briefs*, Vol. 58, Iss. 1, pp. 31–35, (January 2011), **(50 %)**
11. [**MJ MIN/MAX**] R. Długosz, T. Talaśka, "Low Power Current-Mode Binary-Tree Asynchronous Min/Max Circuit", *Microelectronics Journal*, Elsevier, Vol.41, No.1, pp.64–73, (January 2010), **(60 %)**
12. [**NEUR LUK**] R. Długosz, W. Pedrycz, "Łukasiewicz Fuzzy Logic Networks and Their Ultra Low Power Hardware Implementation", *Neurocomputing*, Elsevier, doi:10.1016/j.neucom.2009.11.027, Vol. 73, Iss.7-9, pp.1222–1234, (March 2010), **(80 %)**
13. [**PE MIN/MAX**] R. Długosz, T. Talaśka, "A Power-Efficient, Current-Mode, Binary-Tree Min / Max Circuit for Kohonen Self-Organizing Feature Maps and Nonlinear Filters", *Electrical Review* (Przegląd Eletrotechniczny). At the time of publication the journal was on Thomson Master Journal list, ISSN 0033-2097, R. 86 NR 11a/2010, pp.237–241 (November 2010), **(60 %)**
14. [**EL PD**]R. Długosz, K. Iniewski, "High precision analogue peak detector for X-ray imaging applications", *Electronics Letters*, Vol. 43, Issue 8, pp. 440–441, (12 April 2007), **(80 %)**
15. [**MIXDES AFE**] R. Długosz, "Asynchronous Front-End Asic For X-Ray Medical Imaging Applications Implemented In CMOS 0.18μm Technology", *15th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Poznan, Poland, pp.627–632, (June 2008), **(100 %)**
16. [**MJ MUX**] R. Długosz, P.A. Farine, K. Iniewski, "Power Efficient Asynchronous Multiplexer for X-Ray Sensors in Medical Imaging Analog Front-End Electronics", *Microelectronics Journal*, Elsevier, Vol. 42, Iss. 1, pp.33-42, (January 2011), **(75 %)**
17. [**SPR PSF**] R. Długosz, R. Wojtyna, "Novel CMOS Analog Pulse Shaping Filter for Solid State X-Ray Sensors in Medical Imaging Systems", Chapter 16 in *Computers in Medical*

Activities, Book series: Advances in Intelligent and Soft Computing, ISSN: 1615-3871, ISBN: 978-3-642-04461-8, Vol. 65 / 2009, pp. 155-165, Springer-Verlag, Berlin / Heidelberg, (2009), **(80 %)**

4.2 Description of the publications indicated as the mono-thematic cycle entitled: "Analog and Analog-to-Digital Reconfigurable Low Power Integrated Circuits Working in Parallel and/or in the Asynchronous Fashion"

In the works listed above there are presented investigation results obtained in several areas related to the design of low-power integrated circuits. The works include the design of analog filters, analog-to-digital converters, artificial neural networks as well as systems for the applications in nuclear medicine. Despite this diversity of applications and solutions, all of these systems fall within the scope covered by the mono-thematic achievement entitled as above. The presented filters realized both in the voltage and the current mode technique allow for the parallel and asynchronous work. These circuits are also programmable. By programming their coefficients it is possible to obtain different frequency responses of the filters. The analog-to-digital converters enable parallel operation when their interleaved structures are considered, also designed by the author and described in his presented works. These circuits are also programmable. For example, there exists a possibility to obtain different numbers of the calculated bits at their output. In neural networks, in design of which author participated, both the asynchronous and parallel techniques were always used. Use of these techniques was one of the main advantages of these circuits. A similar approach has been applied in case of the circuits designed by the author for the application in nuclear medicine. In these systems the parallel and asynchronous solutions have to be used, which is caused by the specific data processed by them. All of these systems, as shown below, are often based on similar solutions which proves their versatility. In most of them the author used similar optimization techniques.

4.2.1 Introduction

Series of publications mentioned before, show achievements of the author, including those in which the author's contribution is large, related to the development of new circuit solutions or optimizing the existing ones in terms of their effective implementation in specialized, reconfigurable, very low power integrated circuits operating in parallel and/or in an asynchronous fashion. Asynchronous work is here understood in several ways. On one hand, this term covers systems in which there is no need for a control clock system (p.4.1.[4, 12]). The second group includes solutions in which a circuit during a single clock cycle performs asynchronously several different elementary operations (p.4.1.[2, 6, 11]). The author also includes to the asynchronous circuits those in which particular operations are synchronized using the internal clock, which is triggered by an event. The role of the clock relies, in this case, on serializing a typically short list of tasks, after which the clock block is automatically turned off (p.4.1.[Ref mjMUX, 15], p.5.1.[ref cceceADC]). In this case, the generated clock signals do not need to be good quality. Such assumption for asynchronous mode significantly simplifies the structure of the resultant chip, which in turn leads to substantial savings in power consumption and minimizing the occupied area compared to the analog systems of this type described in the literature.

Application Specific Integrated Circuits (ASICs) due to many advantages are used in almost all areas of modern life. Currently, the largest group are systems based on digital technology, which is due to several important reasons. Technological progress allows for a growing miniaturization, which is in particular important when viewed from the perspective of digital circuits. These systems compared with analogue ones are more robust against the technological process and changes in external conditions such as process, voltage and temperature (PVT). In case of digital circuits the PVT parameters mainly influence the rate achieved by the system, but most often do

not change its functionality even when transistors with minimum sizes in a given technology are used (p. 4.1.[16]). In analog circuits we typically observe significantly greater negative effect of the PVT parameters on the behavior of the overall system.

One of the main problems encountered in analog circuits is the lack of matching between transistors sizes (*transistor mismatch*) that occurs during the fabrication process. In newer technologies one can observe an improvement in transistor matching for given areas of transistor gates, but it is not linearly dependent on the technology (p.5.1.[31,p.4.1.[10]). As an example we can consider two current mirrors implemented in the CMOS 0.18 μm and 0.8 μm technologies. If the gate areas of transistors in both technologies are exactly the same, then the threshold voltage mismatch, ΔV_{th} is in the newer technology only twice less than in the older one. To reduce this problem, in analog circuits transistors need to be substantially oversized. As a result, the use of newer technologies to design purely analog circuits, or systems with a predominance of analog blocks it is not always cost-effective. The author dealt with the problem of transistor mismatch in all projects in which he participated, in all designed circuits. Optimizing the circuits from the point of view of the mismatch effect is not a trivial task. A simple oversizing of transistors does not linearly lead to an improvement of the circuit performance. An important factor is the ranges of the input signals. This is discussed in more detail in following Sections (Section 4.2.5).

Other problems that arise when designing analog circuits include a charge injection effect, which affects the accuracy of the read and write in the analog memory cells analog, and the leakage effect which shortens the amount of time the information can be kept in the memory cells without significant distortions (p.4.1.[10],p.5.1.[31]). An important issue is also the mentioned above impact of changes in ambient temperature on the behavior of systems. The author dealt with these problems for most designed systems. The result of these works were various optimization techniques of the circuits. One of the examples is a temperature compensation circuit proposed by the author, which significantly improved the properties of analog counters used in the systems described in (p.4.1.[6,9]). This is discussed in following Sections (Section 4.2.5).

Digital circuits offer a number of advantages which makes that they are used in an increasing number of cases. Still, there are areas in which analog circuits will always be applied. As an example, one can indicate analog-to-digital converters (ADC), which are composed of both the analog and digital blocks. Since using analog blocks in such systems can not be avoided, therefore such blocks have to be optimized. The optimization techniques in this case include development of new solutions or minimization of the influence of the negative phenomena mentioned above. Author while on foreign scholarships dealt with the development of successive approximation register (SAR) ADCs. In systems of this type a very important role is played by the quality of the digital-to-analog (DAC) converter, which provides a reference signal which is then compared in the comparator with an analogue input signal.

There are applications in which analog circuits offer important advantages in the comparison with purely digital solutions. In some situations moving selected signal processing tasks into analog part of the system can reduce the amount of data that will need to be then converted into digital form. An example are discrete analog filters that can be used as antialiasing filters, after which the sample rate is reduced (decimation). As a result, the number of samples that in the next step have to be converted to a digital form is reduced. The author worked on developing such filters for many years. Initially he designed FIR (Finite Impulse Response) and IIR (Infinite Impulse Response) filters working in the voltage mode (SC – switched capacitor technique) (p.4.1.[1,2], p.5.1.[7]). In following years the author also designed different kinds of programmable FIR filters working in the current mode (p.5.1.[56, 46], p.4.1.[4,5]).

An example of systems in which using mostly analog blocks brings large benefits are analog neural networks (p.4.1.[9,10,11], p.5.1.[2,1]), in design of which the author participated. In this case, there is no need to use ADCs, even though the input signals are analog. This is due to the fact that the neural network outputs are digital 1-bit signals provided by the comparators used in

the block that detects the winning neuron (p.4.1.[11, 13]). Other signals such as weight of neurons are no longer used and so there is no need for their conversion.

However, in most situations the optimal solution is to use mixed analog-digital integrated circuits, in newer technologies as much as possible with the majority of digital blocks. Generally speaking, the answer to the frequently asked question, which of these techniques is better is not easy. Each case has to be considered individually.

The use of ASICs enables relatively easy to achieve parallel data processing and a good fit of the structure of the circuit to the realized task. These features enable to achieve data rate to power dissipation ratio (FOM – Figure of Merit) often many times larger than in typical devices such as computers or FPGAs (Field Programmable Gate Arrays) (p.4.1.[16], p.5.1.[4,5]). Most of the systems proposed and realized by the author, or in design of which the author participated, can operate in parallel. A novel approach in these projects allowed in many cases to obtain a much better FOM than in similar systems of this type described in the literature.

ASICs also allows for the use of the above-described asynchronous data processing. The author applied this approach in several systems. This enabled a significant simplification of the structure of such systems and increasing their speed. An example here is an asynchronous parallel analog image filter proposed by the author (p.4.1.[3]). Another example is an asynchronous parallel analog multiplexer for the application in ASICs used in medical imaging (p.4.1.[16]). The role of this circuit was to capture events occurring at random time instants at particular channels connected to the inputs of the multiplexer. This circuit after a modification, can also be used as an analog non-linear MIN/MAX filter, or as a component of neural networks used to detect winning neuron (p.4.1.[13]).

Low power dissipation and small sized achieved in the systems developed by the author allow for their use in Wireless Sensor Networks (WSNs) and Wireless Body Area Networks (WBANs). One of the key parameters in such networks is the energy consumed by particular nodes. For this reason, the aim of the optimization is the reduction in the power dissipation of particular building blocks of such nodes to allow for their work with the energy drawn from the environment, or a long operation without battery replacement. Typical blocks that are part of the devices used as nodes in WSNs and WBANs include: sensors, filters, ADCs, optional dedicated microprocessor optimized for specific tasks, and the radio frequency (RF) communication module that enables data exchange with other network nodes and the base station. An appropriate optimization of the learning algorithms of neural networks can lead to the profitability of using for data processing miniature neural networks (NNs) directly in WSN nodes. Such NNs would decide when to communicate with the base station. As a result, the communication with the base station would be more seldom, which would save large amounts of energy (RF block often uses up 90-95 % of total energy). The possibility of the development of such systems was the motivation for the study in which the author participated.

The merit part of the presented application is divided into several parts. In next section author presents a discussion concerning the comparison between the voltage and the current modes in the context of his proposed solutions. Such analysis was performed in case of each developed circuit. The aim was to choose the optimal mode viewed from the perspective of the functionality of the system, the type of prevailing mathematical operations in particular cases and the system parameters. In following Section the author presents advantages and limitations of using asynchronous data processing in the circuits in realization of which he participated.

All systems developed by the author or in design of which he took part were designed in the "full-custom" style. For this reason, a short section is devoted to the advantages of circuits design in this way, due to the frequent comparison of this approach with various automatic methods.

Last section presents publications which are part of the main achievements presented in the application. They have been grouped thematically in the chronological order in which individual projects have been implemented. This order results from the fact that many of the solutions

developed in one group of the realized projects after some modifications were subsequently used in the following projects. Sequentially author discusses the works related to the implementation of analog filters (linear and non-linear), analog-to-digital converters, neural networks as well as systems for the applications in nuclear medicine. Because of large number of projects realized in a relatively short period of time (mainly during the author's stay in foreign academic programs), not all realized systems have been verified by measurements. Some projects ended at the transistor level simulations. In the author's opinion, measurement verification was not always necessary, due to several reasons. For example, non-linear MIN/MAX filters operating in the current mode has not been directly verified by measurements. However, almost the same solution was used later in time in the prototype analog WTA NN (experimentally verified), as a building block used to detect the winning neuron. A similar approach was also used by the author to implement an analog Łukasiewicz NN. This network has not been verified by measurements, however, the results obtained in the WTA NN allow high extent assess to the behavior of the Łukaszewicz NN. Some of the realized circuits were based on elementary operations which have been used in other applications described in the literature.

Implementation of the proposed solutions as integrated circuits was also not always possible. The author grant's budget was not sufficient to cover the cost of production and the verification of all solutions. During the scholarships the author was often simultaneously involved in other projects resulting from cooperation with industry, both in Canada and Switzerland. An example here is the participation (in Switzerland) in works that aimed at development of MEMS gyroscope. The author designed the entire feedback loop of the gyroscope containing ADC based on sigma-delta modulator with a decimation filter (5.1.[11]), PID controller and the block that directly generates control signals for the MEMS part. It was a valuable experience, but the results of this work could not be fully published because of the confidence agreement. This cooperation consumed a considerable amount of time that was missing later.

4.2.2 Current mode vs. voltage mode circuits

An efficient implementation of the analog circuits required an answer to the question: Which of these modes is better in particular cases. It is widely believed that systems operating in the current mode feature less precision than systems operating in the voltage mode. Analyses conducted recently, however, show that with decreasing supply voltage that results from the development of the CMOS technology, the advantage of systems operating in the voltage mode is gradually disappearing. At lower supply voltage the maximum amplitude of the signals is reduced, which for a given noise level reduces the signal-to-noise ratio (SNR). Moreover, even if the SNR is in the voltage mode larger than in the current mode, there are systems in which less precision is acceptable, while the advantages of using current techniques are much more important.

Advantages of using circuits working in the current mode:

a. In circuits with a predominance of summation add subtraction operations, current mode circuits offer simpler structure. The result is a smaller area occupied on the chip. This allows for lower fabrication costs and the ability to implement larger systems in a smaller area. Examples are realized by the author SAR ADCs operating in the current mode (4.1.[6, 7, 8]) and filters based on Gilbert multipliers (4.1.[4,5]).
b. For a given supply voltage the current mode circuits are able to work with currents that can vary by up to 1-2 orders of magnitude. The result is a greater flexibility in matching the required speed of the system to the power dissipation. The author observed such properties in the implemented analog filters and the ADCs. However, at this point it is necessary to take into account the fact that with decreasing values of the currents the circuit becomes slower due to longer charging/discharging time of the parasitic capacitance associated with

particular transistors in the current mirrors used in the circuit. As a result, the energy used to perform particular operations decreases only moderately. At very low currents also decreases the accuracy of the system.

c. Easy to implement the "power down" function. In case of the circuits realized in the current mode in the CMOS technology it is usually sufficient to turn off the input signals, to substantially increase the resistance of the channels of transistors in the current mirrors. This substantially reduces the power consumed by the system.

The described advantages of the current mode circuits were crucial in deciding which technique to use in the implementation of the realized analog circuits. It is worth mentioning here that these were the systems for which precision that allows for the effective resolution of signals at the level of 6-8 bits were in most cases sufficient.

Systems operating in the current mode are not free from disadvantages, and therefore require careful design. Below are the potential problems that appear in the design of such circuits and potential ways of dealing with them:

a. One of the main problems is the influence of the mismatch effect of transistors on the parameters of the current mirrors. This impact, resulting from the technological process, is particularly visible in the subthreshold operation of transistors in the current mirrors (p.4.1.[4, 5, 10]). Various design techniques of the structure of the integrated circuit are used to minimize the influence of this effect. A proper placement of transistors in the chip allows for reduction of systematic errors, while an appropriate selection of the sizes of transistors enables a reduction of random errors.

   It is important to ensure that transistors which belong to particular current mirrors are located close to each other and properly arranged relative to each other. It is not always possible. For example, in multi-output current mirrors used by the author in SAR ADC converters, some transistors were not located in the closest proximity. Nevertheless, a two-stage approach to the implementation of the DAC, proposed by the author, enabled in this case a reduction of the area of the DAC by 80 %. As a result, the distances between all transistors have been greatly reduced. Simultaneously there was no need to reduce the sizes of the smallest transistor in the system, which was important from the point of view of the accuracy of the copying operation of signals performed by the current mirrors (p.4.1.[8]). It is described more detailed in Section 4.2.5.

   Another optimization technique relies on oversizing the transistors being part of the current mirrors. However, this approach has a negative impact on the area of the circuit and data rate, which results from increased values of parasitic capacitance of transistor gates (p.4.1.[9, 13, 5]). Analysis performed by the author during designing the circuits described above shows that for a given level of the processed signals, increasing the sizes of transistors does not help and even leads to reduction of precision (p.4.1.[11, 12, 10]). This happens when the transistors operate above the threshold voltage. In this case the gain error of the current mirrors depends not only on the parameters such as, for example, the threshold voltage V_{TH} or the transistor gain factor β, but also on the gate-to-source voltage V_{GS}. If for a given constant range of the applied currents the sizes of transistors will be increased, it will reduce spread of parameters, but also will decrease the V_{GS} voltage, which is enforced by the input current of the mirror. This in turn increases the copying errors. The analysis carried out by the author shows that for a given levels of currents there exists an optimum (intermediate sizes of transistors) that needs to be localized (p.4.1.[10,11,12]). This has been confirmed experimentally in several designed integrated circuits.

b. Charge injection effect has a strong impact on the accuracy of storing and reading operations of the information in the current-mode memory cells. The relationship between the V_{GS}

voltage and the current flowing into the drain of transistor is non-linear (exponential). As a result, for a given range of the operating point of transistors even relatively large changes of the input current cause relatively small changes in the voltage at the gates of transistors used in the current mirror. In sample-and-hold (S&H) memory cell realized as current mirror with a storage capacitor, C_{ST}, and a switch between the gates of transistors, the voltage stored in the capacitor may be affected by the charge injection effect, so it also affects the accuracy of the recorded information.

This problem can be reduced in several ways. One of them relies on increasing the capacity of the storage capacitor, and leaving the sizes of transistors in the switches attached to these capacitors unchanged. Unfortunately, this increases time constants of charging the capacitors, which leads to a reduction in the speed of the circuit. Additionally is enlarges the silicon area. Similar problems the author encountered during the design of analog switched-capacitor (SC) filters operating in the voltage mode.

Another method relies on using the, so called, "dummy" switches. Drains and sources of transistors in such switches are shorted together. The dummy switches are controlled by clock signals of opposite polarity in comparison with the switches used to latch the information in the storage capacitor.

This technique has some limitations. The problem with dummy switches is that in this technique it is very difficult to obtain the linear compensation of the charge injection effect in the overall voltage range (in voltage mode circuits typically 'rail-to-rail'). However, since the voltage stored in the current-mode memory cells varies only moderately with large changes of the input current, the compensation is possible after a proper optimization of the sizes of transistors in the switches.

The author used this technique many times in his projects that include analog filters, memory cells used in analog decoders (5.1.[31]) and his proposed peak detector (4.1.[15]). The experience gained during the development and optimization of these circuits the author used subsequently during realization of analog adaptive mechanism described in (p.4.1.[10]), in design of which he participated.

c. Another problem that has a big impact on the behavior of circuits operating in the current mode is the, so called, leakage effect. This effect can be reduced to some extent by increasing the capacity of the storage capacitor used in memory, but at the expense of reduction of data rate of the system and increase of the silicon area. Another way of reducing the impact of this phenomenon which has been used in the adaptation mechanism described in section. 4.1.[10] relies on such a realization of the analog memory cell to ensure on both sides of the latching switch a similar potential. This technique substantially reduces the leakage effect. The usage of this technique was possible with an appropriate structure of the overall adaptive mechanism that has been used in an analog neural network in the design of which the author participated (p.4.1.[9,10]). This compensation mechanism has been proposed and realized by the author of the application.

In the implemented analog circuits working in the current mode the author did not use active blocks such as operational amplifiers. The aim was to reduce the power consumption as well as the chip area. A disadvantage of this approach was a slightly reduced data rate of the realized circuits. For example, data rate in several circuits realized in the CMOS 0.18 μm technology supplied with a standard voltage V_{DD} of 1.8 V was limited to several MHz. This limitation partially resulted from a relatively small speed of the comparators, realized in this case on the basis of the CMOS inverters. The parameters of such comparators strongly depend on the difference between both compared currents. This problem was observed in circuits described in Section. 4.1.[9-13]. This issue was analysed in more detail during the realization of the parallel circuit used to detect the winning neuron (p.4.1.[11]), proposed by the author. This circuit is described in more detail

later in this application. A similar problem also appeared in the realized by the author nonlinear MIN/MAX filter (p.5.1.[46]) and analog-to-digital converters (p.4.1.[6]).

Taking into account the speed, a better performance was achieved in analog FIR filters operating in the voltage mode when compared to similar filters working in the current mode (p. 4.1. [2]).

4.2.3 Synchronous vs. asynchronous circuits.

Asynchronous circuits potentially pose a number of problems. Some of them occur during the realization of their internal structure, while other during their interaction with synchronous blocks in a larger system. However, there exist areas of application in which the use of such solutions is highly desirable and therefore such circuits should be developed. The way in which the asynchronous blocks collaborate with other blocks is important to ensure the stability of the overall system. Asynchronous circuits can perform a specific list of tasks, working, for example, in the 'feed-forward' mode, in which the overall list of tasks is performed in a single clock cycle imposed by the system.

An example here is the aforementioned ADC realized by the author. In this case, in a single clock cycle the ADC reconfigures the digital-to-analog converter (DAC) throughout a set of switches that modifies the value of the reference current at the input of the comparator. In the same clock cycle this signal is compared with an analog input signal and finally, also in this clock cycle, an appropriate digital block is reprogrammed (p.4.1.[6, 8]).

Circuits of this type can also work as standalone blocks, such as proposed by the author asynchronous parallel image filter (p.4.1.[3]).

Asynchronous circuits can be designed in such a way that in case if an external triggering signal is not active, the circuit is in the "power-down" mode, practically not consuming energy in this time. Once the triggering signal (or signals) becomes active, the circuit goes into an active mode, performs a given list of tasks, and then again goes into the power down mode. An example of such solution is an asynchronous parallel CMOS multiplexer proposed by the author p.4.1.[16] described in Section 4.2.5). In this circuit, the power down mode is achieved in a natural way, as digital CMOS circuits does not consume energy when they are not switched over. The multiplexer has been designed for the application in multi channel specialized ASICs used in nuclear medicine. In such systems, particular channels are activated by data asynchronous appearing on their inputs.

As mentioned earlier to the group of the asynchronous circuits may also be included such solutions, in which a specific list of tasks is performed with an assistance of an internal sequencer. Such sequencer is not controlled from the outside of the circuit but is started and stopped by appropriate internal signals. From the point of view of the external system such circuit is seen as, so called, black box. It is activated under certain circumstances, generating specific results after a period of time not larger than the, so-called, worst case. The period of time referred to as the worst case is here imposed by the external system. The author used such control approach, for example, in the peak detector designed for the application in nuclear medicine. In this case, the internal clock that samples the pulse signal is activated in the moment in which the value of the pulse exceeds a certain threshold (it is signalized by a flag). The clock is automatically switched off immediately after the peak of the pulse is detected (p.5.1.14,15). Once this happens, the overall circuit goes again into the power down mode. In the active mode the sequencer generates a relatively small number of clock cycles. A similar control scheme is also used by the author in one of his ADCs, in which the internal sequencer generated a given number of clock cycles, that controlled particular stages of the conversion algorithm. After completing all assumed conversion stages the ADC was automatically switched off. Such solutions can be classified as the finite state machine (FSM).

Presented asynchronous systems offer several significant advantages. One of them is no need for using a complex external multiphase clock scheme. This greatly simplifies the overall structure of the circuit, for example through the lack of long control lines providing the clock signals.

This in turn has a positive impact on the area occupied by the chip. Circuits of this type consume much less energy. In the analog circuits this also improves the quality of the signal processing, due to the lack of feedthrough of digital clocks signals to analog signal lines. All these features are important from the point of view of circuits used in WSNs and WBANs.

Many asynchronous circuits proposed by the author also enable a parallel signal processing. In some cases it was necessary to ensure a proper management of signals occurring asynchronously in different channels working in parallel. This problem has occurred in the aforementioned circuit designed for the application in nuclear medicine. The role of the manager of these signals held in this case the proposed asynchronous multiplexer. The multiplexer simultaneously achieved a mechanism for the prevention of collisions that could happen if one or more pulses would occur at the same time (p.4.1.[16]).

4.2.4 Designing in the 'full custom' style.

Integrated circuits designed by the author or in design of which the author participated have always been designed in the 'full-custom' style. This method was chosen for several reasons:

a. The proposed circuits contained both analog and digital blocks. Due to the specificity of the realized projects particular components could not always be localized in separate areas. Automated methods such as, for example, standard cells could not be used in this case, as such methods are used to design digital circuits.
b. In the author's opinion, if the "full custom" method is properly used, it allows to obtain better parameters, such as the chip area. An example here is a multiphase clock system designed by the author for the application in analog FIR (finite impulse response) filters working both in the voltage and in the current mode (p.4.1.[2], p.5.1.[63]). Additionally, in many cases designing in the "full custom" style did not take a large amount of time. In such situations using automatic methods would not be profitable.
c. In many circuits implemented by the author or in design of which he participated it was necessary to very precisely determine the locations of particular digital gates or larger blocks in the structure of the chip (p.4.1.[16, 11], p.5.1.[4, 5]). The advantages of these circuits were strongly dependent on the distribution of these elementes in the layout.

4.2.5 Main theses of the publications which are part of the 'indicated achievement'

Publications which are part of the main achievement have been grouped thematically. To this list of publications the author mainly selected those works which were published in top journals and as books chapters. In some cases it was necessary to complement the list of publications by selected conference papers. For example, measurements of the filters based on Gilbert vector multipliers have been published in a conference paper.

1. **Publications devoted to parallel switched-capacitor filters**

   In a series of two papers the programmable, switched-capacitor, finite impulse response (FIR) filter, working in the parallel mode has been presented. The work is a continuation and extension of the author's earlier research on this type of filters, where he designed, fabricated and verified by measurements several prototype filters based on other architectures (p.5.1.[7]). The concept of the filter with circular memory and its preliminary simulation-based verification in the CMOS 0.35 mum technology were presented in the first of the two papers, where he was the only author. In the second paper, a similar filter has been presented, but this time designed in the TSMC CMOS 0.18 mum technology. The project ended up on the

simulation phase, however, the basic operations on which it was based are identical as in previous projects of integrated circuits verified by measurements.

MIXDES FIRSC / SPR FIRSC

In the proposed filter architecture the author eliminated a number of inaccuracies which are present in other architectures of these filters. As mentioned earlier, one of the major problems associated with the analog memory cells are inaccuracies of the read and write operations, which becomes especially visible in the case of multiple rewriting operations of signal samples between memory cells. In the proposed architecture, the number of read/write operations has been reduced to a few only, regardless of the length of the filter. A similar architecture is the one with the, so called, rotating switch. However, in this case, particular memory cells in the delay line are in successive clock phases connected throughout the rotating switch to different capacitors in the output stage of the filter. The usage of the rotating switch has several drawbacks. The switch occupies a relatively large area, which increases with the square of the filter length. In addition, the paths connecting the memory cells to particular capacitors in the output stage are of different lengths, i.e. they have different parasitic capacitance that affects the values of the filter coefficients. In the filter proposed by the author, this problem has been eliminated. The rotating switch has been eliminated, while particular memory cells are always connected to only one capacitor, with programmable value, in the output stage. The effect of moving the samples in the delay line is now realized by moving the capacitance values between adjacent capacitors. Capacitance values of particular capacitors are programmed throughout n-bit signals, which are stored in digital memory. As a results, only digital signals are rewritten between memory cells, which does not affect the quality of analog signals.

The proposed filter can be programmed in several ways. One of them relies on programming the frequency response of the filter throughout programming the values of particular coefficients. Realization of negative coefficients is possible by an appropriate connection (throughout configuration switches) of the coefficient capacitors to the output operational amplifier. The role of this amplifier relies on summing charges of particular coefficient capacitors in the capacitor located in the negative feedback of the operational amplifier. It is worth noting that the values of the products of particular signal samples and the filter coefficients are represented by charges stored in particular coefficient capacitors. In addition, by using several programming signals the filter can be divided into two independent FIR sections, which can be connected in series. With appropriately selected values of particular coefficients the attainable steepness of the pass-band, as well as and the attenuation in the stop band of the filter can be substantially increased. Two separate sections may be combined in such a way that form the infinite impulse response (IIR) filter, which makes the filter even more universal.

The filter operates fully in parallel. storing of successive samples of the signal in the delay line is performed sequentially, but the subsequent multiplication of each sample by the filter coefficients and the summation is carried out fully in parallel. The values of the filter coefficients are rewritten between the capacitors are rewritten also in parallel.

2. **Publications devoted to parallel switched-current filters for the application in image processing**

The continuation of the works on analog filters operating in the voltage mode were realized by the author the FIR filters and the filter banks operating in the switched-current (SI) mode. Two conference papers on this subject have been published, in which the author was the only author (p.5.1.[56,46]), which introduced the concept of the family of the SI FIR filters and the banks of such filters. During the continuation of these works the author developed FIR filters based on the Gilbert multipliers for the application in image processing systems. He also proposed concepts of non-linear filters working with discrete time signals and nonlinear image filters (p.5.1.[45]). The non-linear filters were then further developed as circuits for the application in analog neural networks, as presented in the following sections of the proposal. On the other hand, some solutions used linear FIR SI filters , described in (p.5.1.[56,46]) were then used in the peak detector described in (p.4.1.[14,15]).

As part of the Indicated Achievement the author selected the works devoted to image filters, in which he partially applied earlier solutions. In a series of three publications he presented the concept as well as the implementation, in the CMOS 180 nm technology, of a programmable, analog, asynchronous and parallel FIR filter based on vector Gilbert multipliers working in the current mode. The filter can be used for fast filtering of the images, in which all image pixels are computed fully in parallel. By using the adaptation mechanism, these filters can be used at one of the stages of computing convolution neural networks. The prototype of the filter has been verified by measurements.

MIXDES GVM

The concept of the filter, fully developed by the author, as well as the preliminary verification based on transistor level simulations is presented in the first paper from this series (p.4.1.[3]). The idea of these circuits have been proposed during the author's work on analog decoders (p.5.1.[31]), in which vector Gilbert multipliers were commonly used (cooperation with Prof. Vincent Gaudet). The author noted that these circuits offer features that can be used to implement parallel and asynchronous FIR filters. Preliminary simulations have shown that, in theory, such filter can process up to several hundred thousand frames per second without using a controlling clock generator. In the paper the author limited his investigations to an image with a resolution of 8x8 pixels only. This resolution may, however, be easily increased by simply duplicating particular blocks. The proposed filters are programmable, which means that they enable realization various frequency responses, both the low pass and high pass with different coefficients. Programming of the filter is carried out with only a few dozen bits. The programming process is so fast (several tens of nanoseconds), that it can be done even during the operation of the circuit. The paper presents simulations for both the low-pass and the high-pass filter. These filters can be an alternative to cellular neural networks used in image filtering.

SPR GVM

In the following paper in this series there have been presented two versions of this filter that enable operation with the signals sampled in the time domain (1-D) and sampled in the image coordinates domain (2-D). In the first case, a clock has been used, but only for storing consecutive signal samples in the delay line, while further signal processing was executed fully in parallel and asynchronously. In the second case (2-D signals) the filter operates fully asynchronously and fully in parallel. This means that all input signals can be supplied to the circuit continuously, without sampling. The filtered samples appear at the outputs of the filter after a delay that resulted only from the circuit's structure. In the simulations, these

delays did not exceed 1–10 μs, depending on the levels of the input currents, which could be scaled in a fairly wide range.

BIODEV GVM

The third paper presents the practical realization of a prototype image filter in the TSMC CMOS 180 nm technology. The structure of the integrated circuit has been completely designed by the Author, who then also made the measurements of the fabricated chips. In measurements the delays were higher at the level of 20–100 μs, which resulted from high capacity of the pads. In the chip the author designed three filter with the same scheme but with different sizes of transistors. The purpose was to investigate the impact of mismatches between transistors on the filtering accuracy. Depending on the noise observed during measurements, and the levels of the input currents, the effective resolution of the filter was 6 bits (for the largest currents). It is worth noting that the maximum tested currents were at the level of about 6 μA, while theoretically it is possible to work with the currents of up to three times higher.

The measurements as well as the simulation results show that, theoretically, for the image resolutions at the level of 1 MPixel cooperating with, for example the CCDs or CMOS sensors, one can obtain the computation power of the order of several to several tens GPixels /s. The bottleneck here is the need to provide large amounts of data to the system and later to collect the results. One of the possible solutions of this problem is the use of 3-D ASICs, which allow for a larger number of pads placed not only on the ring of pads.

3. **Publications devoted to analog-to-digital converters**

One of the important areas of interests of the author are algorithmic ADCs that operate on the basis of the SAR architecture (successive approximation register). Many papers have been published in this area in the world, mainly presenting converters operating in the voltage mode, based on charge-redistribution architectures. The author in his investigations went in another direction. His goal was to achieve a very small area of the circuit, to enable using of many such converters in a single chip. This feature is of large importance in artificial neural network operating in the mixed analog-digital mode, but also in circuits used in nuclear medicine (p.4.1.[7]). Converters of this type can also be used in large integrated circuits to perform a control measurement of selected analog signals. In this case, to the outside of the chip are provided digital equivalent signals of of the measured analog signals.
To achieve a small chip area the author realized his circuits in the switched currents technology. As a result, it was possible to substantially reduce the area of the DAC (digital-to-analog converter) which is one of the components of the SAR ADC. As a result, the author designed a reconfigurable 10-bits ADC (in the cooperation with the IHP Institute in Frankfurt Oder in Germany) in the CMOS 130 nm technology. The ADC occupies the area of only 0.01 mm^2. This means that it is probably the smallest circuit of this type in the world.

The results of these investigations have been presented in several publications. Selected works are part of the presented indicated achievement.

VLSIDES ADC

First of the publications in this series (p.4.1.[6]) presents the concept of an 8-bits SAR ADC realized in the TSMC CMOS 180nm technology. It also presents the converter working in the time-interleaved architecture, in which eight single SAR ADC sections operate fully in parallel. The second circuit allows to adjust, in a wide range, data rate and the resolution of the output signal, while the power dissipated by the circuit is always well fitted to the computation power of the ADC. In a single section ADC there exists the possibility to program the controlling

clock system, while the time-interleaved version allows also for disabling sections unused at a given moment. The last feature has a big impact on the possibility to change the resolution of the ADC and data rate.

The clock circuit used in the ADC was based on the analog counter connected to the temperature compensation circuit proposed by the author. The compensation circuit enabled a large flexibility of the clock system with the modulo varying over a wide range, working stably even for large changes of the temperature. This circuit after a modification was then used in the conscience mechanism designed for the application in analog Kohonen neural network, in design of which the author participated (p.4.1.[9]).

In subsequent works in this area the author proposed the concept of a two-stage DAC (digital-to-analog converter) working in the current mode. The concept of this system has been described in book chapter published by CRC Press (p.4.1.[7]) and then realized in the form of a prototype chip described in (p.4.1.[8]).

CRC ADC

Second work in this series is the book chapter. Due to the fact that works of this type are often tutorials, therefore in much larger extent than in other works the author focused on the literature studies in this area. The author in his investigations analysed and compared the parameters of several hundreds ADCs based on various architectures (selected cases are presented in the publication). In this work the author presented the concept of a new current-mode SAR ADC with two-stage DAC. The concept has been widely discussed in the next work described below.

MIXDES ADC

The proposed concept of the current-mode two-stages DAC is of great importance for the improvement of the overall circuit parameters. In case of a single-stage approach the DAC is implemented on the basis of a multi-output current mirror, in which the widths of channels of particular output transistors change with the power of 2. This means that in the 8-bits version of the ADC the width of the largest transistor is 128 times larger than in the smallest one. To minimize the impact of transistor mismatch the smallest transistor has to be oversized. However, this means that the sizes of the largest transistors become very large in this case. In the case of two-stage approach dispersion of the channel widths can be much smaller, while an important is the product of the gain factors in corresponding branches in both stages of the DAC. Implementation of the ADC based on this concept in the CMOS 130 nm technology is described in the third of the presented works from this series (p.4.1.[8]). The chip containing this ADC has been designed during the author's stay in the IHP Microelectronics Institute in Frankfurt Oder under the framework of the DAAD scholarship. This year the project of the chip was sent to the production in the IHP.

The application of the concept of the two-stage DAC enabled to design the ADC with a resolution of n=10-bits, which occupies the area of of 0.01 mm^2. A good linearity and precision of the DAC has been obtained by using cascoded mirrors. For data rate of 0.55 Msamples/s and the resolution of 10-bit the circuit dissipates an average power of 13.2 μW (simulation results). Figure-of-Merit (FOM) calculated as FOM = $P/(2^n \cdot f_S)$ is one of the lowest of the reported in the literature. The results are shown in a Table in the paper (p.4.1.[8]).

The circuit is programmable. The two-stage DAC consists of ten branches that generate components of the reference current I_{REF}, depending on the value of particular control bits calculated by the ADC in subsequent stages of the approximation algorithm. If the lower resolution is sufficient, one can select the branches that will be used. This allows for a control

of the speed of the ADC in a large range and simultaneously adjust the power dissipation to the realized task.

One of the problems was an appropriate control of the currents of particular branches in the DAC, which are components of the reference current I_{REF}. Theoretically, one of the possibilities is switching off selected branches by a set of switches if their corresponding bits are 0. However, the problem that arises in this case, are long periods of times a given current needs to disappear and to occur during switching off and on of a given branch. To avoid such a situation the author proposed a solution in which particular currents are not switched off, but only switched over to additional current mirrors controlled by switches with opposite polarity. As a result, switching on/off of branches that carry even large currents takes as much time as the ones with small currents. This approach was crucial to achieve a relatively large data rates at given levels of the power dissipation.

At the moment there are only available the results of postlayout simulations of the ADC (corner analysis) and the analysis of the negative effects that allowed to select optimum sizes of the transistors for the assumed ranges of the currents. The circuit currently is in the production phase and will be verified experimentally later. However, the circuit to a large extent is based on the solutions used by the author previously in other circuits that have been positively verified by measurements.

4. **Publications devoted to artificial neural networks implemented in hardware**

Artificial neural networks implemented in hardware is another research area in which the author actively participated. The works in this area were mostly realized in a team, which resulted from the complexity of the implemented circuits and larger systems. However, there exists a possibility to clearly indicate the solutions proposed by the author. These solutions were very important from the point of view of the quality of information processing performed by the neural network. The author of the application also performed a series of studies aimed at optimizing the systems included in these networks. The author selected five publications on this topic, in which his participation was significant or dominant.

First three works are related to the implementation of an innovative analog self-organizing WTA (Winner Takes All) neural network realized at the transistor level in the CMOS 180 nm technology. The network operates in parallel, and most operations are performed asynchronously.

All major building blocks of this neural network has been designed from scratch by the participants of the project. The use of existing solutions was impossible, since particular blocks had to perform specific functions not found in other solutions. The author of the application has been actively involved in the design of each component (in some cases his participation was dominant). Details are presented below, but also in declarations of particular participants that took part in this work attached to the application.

TNN CONS

In the first of the papers in this cycle has been presented the, so called, conscience mechanism, which in the WTA neural networks is used to reduce or fully eliminate the number of the, so called, dead neurons. The circuit in the version presented in the paper consists of three basic building blocks, such as an analog counter that counts the number of the wins of particular neurons, the temperature compensation circuit, as well as the converter of the voltage signal stored in the counter to an equivalent current.

The author of the application completely independently designed the temperature compensation circuit used to stabilize the analog counter. A similar compensation circuit has previously been used by him in the analog-to-digital converters, described in (p.4.1.[6]). The

author also modified the analog counter, proposed earlier by Dr. Talaśka, to enable a direct connection of the gate of the MP2 transistor in the counter (Fig. 3 in the paper) to the control signal coming from the compensation circuit. This allowed to eliminate the impact of variability of parameters of the intermediate elements (NOT gate or switch), which in earlier versions of the counter were at the input of the MP2 transistor. This improved the quality of the temperature compensation. A similar control scheme has been used in the analog-to-digital converter described in (p.4.1.[6]). The control scheme proposed by the author is that the width of the impulse signal that opens the MP2 transistor is modified depending on the temperature. If for example, due to temperature variation, the current charging the C_2 capacitor becomes higher, then similar higher current also flows through the C_1 capacitor in the compensation circuit (transistor MP1 in this circuit has the same sizes as the transistor MP2 in the counter). As a result, the signal at point D in the compensation circuit reaches the logical value '1' in a shorter time, which results in an earlier reset of the ENt signal. In this way, the amount of charge which for a single ENt impulse flows into the C_2 capacitor is almost independent on the temperature. The control mechanism and the compensation circuit proposed by the author played an important role in achieving by the overall conscience mechanism good performance.

The role of the author in this paper was also the analysis of the impact of negative effects, such as transistor mismatch, on the behavior of the circuit. The author dealt with this type of the analysis already earlier, during the realization of analog filters and analog-to-digital converters described above, as well as Łukasiewicz neural network described later.

The author also designed the layout of the proposed temperature compensation circuit in the CMOS 180 nm technology and carried out its detailed verification (corner analysis).

For more details see statements on the participation of particular authors presented in separate documents attached to the application.

TCAS ADM

The second paper in this cycle presents the concept as well as the experimental results of the current mode circuit used for adaptive modifications of neurons weights in analog WTA neural network. The presented circuit features an extended storage time of the information in the memory cells. The concept of the circuit relies on the use of two alternately working memory cells for each weight in the neural network. In one of these cells remembered is the current value of a given weight. If a given neuron becomes the winner, then for each of own weights, $w_{i,j}$, it calculates an update, $\Delta w_{i,j}$, which is then summed up (in the node) with the weight value stored in this memory cell. The result of the summation is saved in the second cell, and the output of this cell becomes a reference point in the next calculation cycle for a new learning pattern X. If this neuron wins once more, the signal stored in the second cell is summed with the calculated new update $\Delta w_{i,j}$, while the result is stored in the first cell again. To enable switching between these two cells is used a simple digital circuit composed of D-flip-flop and several logic gates.

A first version of this circuit has been proposed in the paper (p.5.1.[43]). Main inventor of this circuit was Dr. Tomasz Talaśka and therefore in this form the circuit has been also presented in his PhD dissertation. A disadvantage of the original version was large leakage of the analog memory cells, which causes that the neural network was not able to operate with low sampling frequencies required, for example, in processing of biomedical signals.

Considering the described problems the circuit has been later modified by the author of the application, which proposed a solution that allows for a significant reduction of the leakage effect in memory cells that store the neuron weights. The proposed mechanism to reduce the leakage effect was one of the main innovations described in this paper (it is not present in the PhD thesis of Dr. Talaśka). It allowed for a large extension of the storage time

of the information, which is important for the implementation of large networks operating at low frequencies. In such networks, refreshing of particular weights usually takes place at a lower frequency, so such networks are more sensitive to the leakage effect.

The modification proposed by the author of the application relies on adding to the circuit OR gates that control switches S_{C1} and S_{C2} (Fig. 1 in the paper). The signal S_C fed to one input of both gates act as a parameter (1 or 0). When its value is '1', the current I_1 and I_3 flow whole the time. It strongly reduces the difference of potentials between the nodes (in pairs) A–B and C–D, resulting in reduced leakage currents. If the neural network operates with high frequencies and thus the leakage is small, then the value of the parameter S_C can be set to 0, which temporarily disables the currents I_1 and I_3, causing a reduction in the power dissipation. This makes the circuit very flexible.

The contribution of the author of the application to this work was also a thorough analysis of the mismatch effect. This analysis allowed to calculate optimal sizes of transistors in the circuit, suitable for the assumed ranges of the currents. A simple increasing the sizes of transistors in order to reduce the mismatch could not be used for several reasons. In this circuit, some of the transistors operate in the strong inversion region, while some of them in the subthreshold region. Therefore, the sizes of each group of transistors had to be determined separately, taking into account other parameters of the circuit, such as the variation of ranges of the currents in particular branches and the voltages stored on the capacitors. This was therefore a multi-dimensional optimization, which was a problem itself. A considerable part of the article has been devoted to this problem. The author already dealt with this type of analysis earlier in the optimization of the analog filter based on Gilbert multipliers and SAR ADC described above, as well as in the Łukasiewicz neural networks described later in the application.

The author also dealt with the optimization of the system in order to minimize the charge injection effect. The optimization relies on adding to the circuit aforementioned dummy switches and determination of their sizes. In this task the author based on his previous experience with the design of analog filters and analog memory cells used in analog decoders (5.1.[31]), as well as with his proposed peak detector (4.1.[15]).

It should be emphasized here that the proposed modification of the circuit in order to minimize the leakage effect, the analysis of the mismatch effects, as well as the optimization of the circuit in order to minimize the charge injection effect do not occur in the PhD dissertation of Dr. Talaśka. These are new added values in relation to the original version of the circuit.

The contribution of the author to the presented work was also completely new extensive literature study ("state-of-the-art"). This study mostly concerned minimization of the leakage effect in analog memory cells. Only two works listed in References of this paper were also cited in the PhD dissertation of Dr. Talaśka. This study more closely coincide with one of the earlier author's papers, in which he presented analog memory cells for analog decoders (p.5.1.[31]).

For more details on the contribution of each of the co-authors of this paper in the implementation of the proposed mechanism refer to their declarations attached to the application.

MJ MIN/MAX

The third article in this series presents the concept, as well as the CMOS implementation of an asynchronous, parallel circuit used to detect the winning neuron in the realized WTA neural network. The winning neuron is the one whose output signal that represents the distance between its weights vector and a given learning pattern has the smallest value. Detection of this neuron requires the circuit that performs the $\mathrm{MIN}(d_1, d-2, \ldots, d_M)$ function, where M is the number of neurons in the network. The paper presents a more universal,

programmable, circuit, which can also perform the MAX$(d_1, d-2, \ldots, d_M)$, function together with the circular delay line needed to achieve the functionality of non-linear filters.

The concept of the circuit as a whole proposed by the author of the application is based on an asynchronous binary tree. In the comparison to conventional solutions of this type, the author proposed a modification that eliminates the accumulation of errors that typically occur during the propagation of signals between successive layers of the tree. The concept of the circuit comes from the author's previous works on analog current-mode filters, including non-linear Min/Max filters, as well as Łukasiewicz NN described below.

On the basis of the binary tree structure, one can develop circuits that perform the MIN and the MAX functions. Both these functions can be easily implemented in a single circuit. To switch between both functions, for given input signals, it is only required to negate all output signals from the comparators used in the circuit. The proposed circuit offers such a functionality. Both the MAX and the MIN functions are commonly met in non-linear filters used, for example, in the image processing. At this point it is worth noting that the usage of this circuit in neural networks and in the filters is completely different. This fact is often not distinguished in the literature, however it is crucial while comparing parameters of different solutions. In the first case the calculated Min value is not used, while the address of the winning signal (the neuron which provided this value) is the useful information. In the non-linear filters, on the other hand, the situation is opposite. In this case the address of the Min/Max signal is not important, while the useful information is the value of this signal. This causes that the MIN circuits designed for the application in neural networks are typically more complex. In practice, the only way to implement such circuit in this case requires using binary tree with the comparators.

In a typical binary tree the signals provided to particular inputs of the tree compete with each other in pairs in blocks, which in the paper are denoted as MIMA2. Each of these units comprises a comparator, which with a single output bit indicates a local winner. The winners of each pair are copied to the next layer of the tree, in which a second round of the competition takes place. This process is repeated for subsequent layers. In each successive layer the number of the MIMA2 blocks is halved in the comparison to the previous layer. The last layer of the tree contains only one MIMA2 block that determines the winner from all input signals. The address of this signal is determined by an appropriate asynchronous logic block on the basis of the output signals from particular comparators.

In typical solutions based on the binary tree concept, described in the literature, the signals from the inputs of particular MIMA2 blocks are propagated to their outputs. Each MIMA2 block typically contains several current mirrors on the path between it's inputs and the output. Each such mirror introduces some error resulting from the copying operation of the current. The errors cumulate in successive layers of the tree, which is one of the main disadvantages of such circuits. In the proposed circuit this problem has been substantially reduced. The propagation of signals from layer to layer has been eliminated, while now each input signal is copied as many times as the number of the layers in the tree. Each of the layers may receive a direct copy of each input signal. Selection of neurons from which the signals are provided to particular layers depends on the competition results on preceding layers. Particular signal paths are configured by means of switches controlled by appropriate combinations of digital outputs signals from the comparators on particular layers. The author used a very similar concept in his another work dedicated to Łukasiewicz neural networks, described below.

The circuit operates asynchronously. After providing new signals to its inputs, after a period of time in which there is a transient state in the circuit, the circuit generates the correct results. Further details are presented in the paper.

It is worth to note in this place that the circuit presented in this paper is based on a totally different approach than the circuit of this type described in the doctoral dissertation of Dr. Tomasz Talaśka. In the circuit presented in the dissertation the signals were propagated between layers of the tree, so that those solutions was one of typical solutions widely described in the literature.

NEUR LUK

In the fourth paper in the series of works devoted to analog neural networks the author proposed a new category of analog Łukasiewicz OR and AND neurons working in the current mode, as well as the entire neural network based on these neurons. The operation of the neurons is based on logic *or* and *and* operations carried out on multivalued input signals. These operations belong to the group of several basic operations used in the fuzzy logic. Hardware implementation of all these operations proposed for the first time Yamakawa in 1986 (reference [15] in the paper). Used in this case *or* and *and* operations are based on the operations, respectively, 'bounded sum' and 'bounded product' that belong to this group.

Yamakawa based his implementation on the current mode technique, which is the most appropriate to implement this type of circuits. This is due to the ease of obtaining summation and subtraction operations, which dominate in this case. The disadvantage of his implementation is, however, a potentially large decrease in the accuracy of signal processing resulting from the mismatch of transistors in the current mirrors (see Section 4.2.2). The problem becomes particularly noticeable when between the inputs and the outputs of larger system there is located a number of current mirrors connected in cascade, which leads to accumulation of copying errors.

In the paper the author first proposed a hardware implementation of the neural network based on the original Łukasiewicz fuzzy operations proposed by Yamakawa. In this case, the minimum number of current mirror between the inputs and the output of the circuit was six. In the next stage the author proposed its own implementation of the OR-AND and AND-OR network, in which he used multi-output current mirrors, simple current comparators, and switches controlled by appropriate combinations of digital signals from the outputs of the comparators.

The operation scheme of the circuits proposed in this paper is very similar to the one of the MIN/MAX circuit described above, presented in (**MJ MIN / MAX**). Multi-output current mirrors generate several copies of the input signals. Particular copies are fed to subsequent calculation stages of the overall circuit by means of the switches. One copy of each input signal is also provided to the output of the overall neural network, which means that between the inputs and the outputs of the circuit there is only a single current mirror. Looking from the pont of view of the accuracy of signal processing this is one of the main advantages of the proposed solution.

The proposed neural networks operates fully asynchronously without necessity of using a controlling clock circuit. Data processing is performed in parallel regardless of the number of the input signals. As a result, the circuit depending on the input values can achieve high computing power with a relatively low power dissipation. In transistor level simulations carried out in the CMOS 180 nm technology the circuit worked properly for the maximum value of the input signals changing in the range of tens of nA to 10 μA. However, it must be remembered that for small currents operating points of particular transistors are in the subthreshold region, which affects the accuracy of the overall circuit. For this reason working with small currents is not optimal.

The main aim of this paper was to present the concept of a new circuit. This required introducing appropriate relationships describing the circuit, and verification of the assumptions on the basis of simulations in SPICE. Although experimental verification has not been

carried out in this case, but the results were affected by similar errors as in the case of the MIN/MAX circuit described above (**MJ MIN / MAX**), which has been verified also by measurements.

PE MIN/MAX

The fifth paper presents a novel system with functionality similar to the MIN/MAX circuit described in the previously presented study (**MJ MIN/MAX**). In the previous circuit it has been eliminated one of the major drawbacks of systems based on binary tree structure that is the accumulation of copying errors between the layers of the tree. Nevertheless, the overall signal processing is performed using the analog circuits. Particular MIMA2 blocks include analog comparators, that receive signals provided by current mirrors. The accuracy of the system is therefore to some extent affected by the mismatch effect of transistors described in papers **TCAS ADM** and **NEUR LUK**. One of the problems is also the fact that the negative inputs of the comparators receive the input signals throughout two current mirrors, while the positive inputs by only one. This can be a source of offset phenomena occurring at the inputs of the comparators.

In this article, it has been proposed a new MIN/MAX circuit based on a different concept. Since this circuit has been also designed for the application in neural networks, therefore is has to be able to determine the address of the winning signal. For this reason, the concept of the binary tree has been used once more, but in this case, the tree consists of only digital blocks.

At the inputs of the overall MIN/MAX circuit are used current-to-time converters (ITC), proposed by the second co-author of the paper - Dr. Tomasz Talaśka. The input currents charge the capacitors connected to the CMOS inverters. Particular inverters switch after the time proportional to the respective currents, generating the output digital signals (flags) delayed for specified periods of time. Further signal processing is performed in the digital binary tree proposed by the author of the application. In the tree there have been used circuits which are able to determine which of the input flag at input appeared earlier or later (depending on whether the system performs the function MAX or MIN).

The author of the application proposed two versions of the binary-tree circuit, for the MAX and the MIN functions, respectively. In the first case when a given T_CMP (*Time Comparator*) which is part of the binary-tree structure, receives one of the flags, the block almost immediately sends the flag to the second layer of the tree. The delay is equal to the propagation time of only one logical OR gate. At the same time, in parallel, the T_CMP circuit performs a competition between two input flags. The second layer of the tree sends its flag to the next layer, and so on. The process for the tree containing 7–8 layers takes only several ns CMOS 0.18 μm. In the T_CMP circuit operating in the MIN mode AND gates are used instead of the OR gates. The AND gate sends its flag to the next layer only when it receives both flags.

One of the advantages of this MIN/MAX circuit is that all the ITC blocks have the same structure. For keeping the lengths of all paths equal, the system can be very accurate. The issue here is how to assure the same resistances and parasitic capacitances of particular paths. In Section 4.2.1 of the application, the author wrote that in digital circuits the PVT parameters mainly affect their speed. It may be added here, that transistor mismatch has also some influence on data rate achieved in such circuits, especially if transistors with minimum sizes in a given technology are used. Differences in data rates of particular T_CMP blocks theoretically can cause off-sets in the comparators. This effect is, however, negligible in this case, as transistors used in particular current mirrors have been substantially resized, which minimizes the impact of the mismatch effect.

The concept of the digital binary tree has been proposed by the author of the application. This concept has been originally used in asynchronous multiplexer designed for the application in circuits used in nuclear medicine, originally published in (p.5.1.[44]), and then after an optimization in the paper (MJ MUX) described later in this Section of the application. This shows that the system is universal. It can be used as a non-linear filter (MIN or MAX), a system for selecting the winning neuron in neural networks (only MIN) and applications related to nuclear medicine (MAX function). The difference between the applications relies on using (or not) the delay line at the input. This line is used only in case of non-linear filters.

5. **Publications devoted to circuits used in medical imaging**

The author of the application was also involved in development of circuits that find the application in ASICs used in medical imaging in nuclear medicine. The obtained results have been published in two journal papers from the Philadelphia List, one chapter in the book published by Springer, as well as in several conference publications. The most important works from this cycle have been incorporated into the presented main achievement of the author. The solutions used in these circuits to a large degree result from previously described works of the author and form with them a whole. These circuit are able to work in parallel and usually also asynchronously. In several cases there exists the possibility of their reprogramming.

EL PD / [MIXDES AFE]

In the first of these papers (**EL PD**) the author proposed the concept of a peak detector (PD), which was then improved by him in the second presented paper from this series ([**MIXDES AFE**]). The proposed peak detector to some degree is based on previous author's works on analog FIR filters operating in the current mode (p.5.1.[56, 46]). The circuit consists of the circular delay line controlled by a 3-phases (in the improved version) clock that is activated asynchronously when the input signal reaches a value exceeding a certain threshold. At the start of the clock the growing signal coming from the pulse shaping filter (PS) is sampled in the delay line. An appropriate arrangement of the switches in the delay line causes that the sample that entered the delay line earlier is always directed to the negative input of the comparator, while the next sample to its positive input. As a result, as long as the pulse rises, at the output of the comparator is a logical value of '1 '. Once the pulse reaches a peak, the output of the comparator becomes '0 'and the peak value is latched in a sample-and-hold (S&H) memory cell. It also turns off the clock generator and switch over the overall channel into the power-down mode.

MJ MUX

In the next paper of this series the author presents a novel parallel and asynchronous multiplexer for the use in ASICs used in medical imaging in nuclear medicine. The role of the multiplexer is to capture events occurring asynchronously in the channels connected to respective inputs of the ASIC. The prototype system of this type with eight channels and supports them multiplexer was then realized in the CMOS 0.18 μm technology.

The concept of the multiplexer the author relied on a similar solution which has been also applied in the winning neuron selection circuit described above (**PE MIN/MAX**). The main advantages of the circuit are very low power dissipation as well as very small chip area. The system normally is in the power-down mode, in which it does not consume energy. If at one (or more) of its inputs appears a flag that indicates that the corresponding channel has detected the pulse, the multiplexer automatically becomes active, laid the path between this channel and the output of the overall ASIC, and then immediately returns to the power-down

mode. It is also important that during laying the path switched are only those blocks (T_CMP circuits described in **PE MIN/MAX**), which are located on this path, while other blocks of this type remain inactive. The process of laying the path is very fast. In the circuit designed in the CMOS 0.18 μm technology it takes less than 1 ns. This result has been obtained for an example system comprising eight inputs, i.e. three layers in a binary tree. This time is growing relatively slowly with the increase in the number of inputs, M, due to the fact that the number of the layers in the tree is only $\log_2 M$ (assuming that M is a number which is one of the powers of 2). It is one of the main advantages of the system.

The circuit comprises a mechanism for prevention of collisions. This mechanism causes that even in the case of the simultaneous appearance of many events, the access to the output of the ASIC has only one channel. After reading out data from this channel the multiplexer automatically switches over to a next active channel. In this way, the information stored in particular channels is not lost. Details concerning the internal structure of the circuit and their operation are presented in the paper.

SPR PSF

This paper presents the concept of a pulse shaping filter operating in the voltage mode, for the applications in ASICs used in medical imaging. The filter has a simple structure. It does not require active components such as operational amplifiers. By modifying the values of particular elements one can modify the response of the filter. The modification relies on adjustment of two voltages. The filter was used in a prototype front-end ASIC implemented in the CMOS 180 nm technology.

4.2.6 Conclusions A summary of the presented series of the publications

The presented series of publications provides an overview of various works and projects in which the author actively participated. Most of these projects is based on novel circuit solutions proposed by the author. In some cases, the author has proposed significant improvements to circuits proposed by other members of the team.

Not all of these projects finished with the implementation of a prototype chips, partly due to lack of sufficient funds. However, it was not always necessary, what was the main reason. Particular concepts of the circuits have been often used in several different projects, some of which completed with a prototype chip and its verification measurements. One of such examples is a temperature compensation circuit, which has been initially used in the analog-to-digital converters to control the clock generator. After a redesign it was also used in the analog WTA neural network that has been verified by measurements. A similar situation was in case of non-linear filters Min/Max participated as well as the Łukasiewicz neural networks, which after modifications have been also used in the same analog WTA network as a circuit used to detect the winning neuron. Another example is parallel programmable SC FIR/IIR filter, which has been verified only by simulation. It was based, however, on operations that author has applied in his earlier projects of such filters verified by measurements.

Many of the proposed solutions is universal. An example here is the circuit that may be used as an asynchronous multiplexer, a non-linear MIN/MAX filter, but also as a circuit used to detect the winning neuron in parallel neural networks.

The common denominator of the presented works is that they present circuits that can operate in parallel and/or asynchronously. In addition, there is a possibility of their programming. These features are relatively difficult to implement in analog integrated circuits. The proposed circuits typically are mixed analog/digital solutions, designed in such a way to enable achieving very low power dissipation.

5 Other research and teaching achievements

5.1 List of other publications published after obtaining the doctoral degree

5.1.1 Articles in scientific journals from the Philadelphia List

1. M. Kolasa, T. Talaśka, R. Długosz, "A Novel Recursive Algorithm Used to model Hardware Programmable Neighborhood Mechanism of Self-Organizing Neural Networks", *Applied Mathematics and Computation*, Elsevier, 2015, **accepted**, http://dx.doi.org/10.1016/j.amc.2015.03.068
2. T. Talaśka, M. Kolasa, R. Długosz, P.A. Farine, "An Efficient Initialization Mechanism of Neurons for Winner Takes All Neural Network Implemented in the CMOS Technology", *Applied Mathematics and Computation*, Elsevier, 2015, **accepted**, http://dx.doi.org/10.1016/j.amc.2015.04.123
3. T. Talaśka, M. Kolasa, R. Długosz, W. Pedrycz, "Analog Programmable Distance Calculation Circuit for Winner Takes All Neural Network Realized in the CMOS Technology", *IEEE Transactions on Neural Networks*, 2015, **accepted**
4. R. Długosz, M. Kolasa, W. Pedrycz, M. Szulc, "Parallel Programmable Asynchronous Neighborhood Mechanism for Kohonen SOM Implemented in CMOS Technology", *IEEE Transactions on Neural Networks*, Vol. 22, Iss. 12, pp. 2091–2104, (December 2011)
5. M. Kolasa, R. Długosz, W. Pedrycz, M. Szulc, "Programmable Triangular Neighborhood Function for Kohonen Self-Organizing Map Implemented on Chip", *Neural Networks*, Elsevier, Vol. 25, pp.146–160, (January 2012)
6. R. Długosz, T. Talaśka, R. Wojtyna, "An Influence of Current-Leakage in Analog Memory on Training of Kohonen Neural Network Implemented in Silicon", *Electrical Review* (Przegląd Eletrotechniczny), Thomson Master Journal list, ISSN: 0033-2097, ISSN 0033-2097, R. 86 NR 11a/2010, pp.146–150, (November 2010), **(30 %)**
7. A. Dąbrowski, R. Długosz, P. Pawłowski, "Integrated CMOS GSM Baseband Channel Selecting Filters Realized Using Switched Capacitor Finite Impulse Response Technique", Elsevier, *Microelectronics Reliability Journal*, Vol. 46, No. 5–6, pp. 949–958, (June 2006), **(50 %)**
8. A. Dąbrowski, R. Długosz, "Comparison of Various SC FIR Filter Structures on the Basis of their CMOS Realization and Simulation in the PSPICE Program", *Bulletin of the Polish Academy of Science. Technical Sciences*, Vol. 49, No. 1, pp. 59–79, (2001) ((this paper was published before obtaining the PhD degree. It is provided here in addition to Table 2)

5.1.2 Remaining papers in national and international journals

1. R. Dlugosz, M. Szulc, M. Kolasa, et al., "Design and Optimization of Hardware-Efficient Filters for Active Safety Algorithms," *SAE International Journal Passengers Cars – Electronic and Electrical Systems*, 8(1):2015, doi:10.4271/2015-01-0152
2. R. Długosz, A. Rydlewski, T. Talaśka, "Novel, Low Power, Nonlinear Dilatation and Erosion Filters Realized in the CMOS Technology" *Facta Universitatis, Series: Electronics and Energetics*, Vol. 28, No. 2, June 2015, pp. 237-249, DOI: 10.2298/FUEE1502237D
3. M. Kolasa, R. Długosz, "Koncepcja Zastosowania Sztucznych Sieci Neuronowych do Lokalizacji Elementów Powodujących Pogorszenie Jakości Energii Elektrycznej w Sieciach Średniego Napięcia", *Poznan University of Technology Academic Journal of Electrical Engineering*, No. 70, 2014, pp.87-95
4. R. Długosz, M. Kolasa, T. Talaśka, J. Pauk, R. Wojtyna, M. Szulc, K. Gugała and P.A. Farine, "Low Power, Low Chip Area, Digital Distance Calculation Circuit for Self-Organizing Neural Networks Realized in the CMOS Technology", *Solid State Phenomena*, Vol. Mechatronic

Systems and Materials V, Trans Tech Publications Inc., Kreuzstrasse 10, 8635 Durnten-Zurich, Switzerland, ISBN: 978-3-03785-645-1, pp.247-252, (March 2013)

5. M. Kolasa, R. Długosz, W. Jóźwicki, J. Pauk, A. Świetlicka and P.A. Farine, "Analysis of Significant Prognostic Factors of Patients with Bladder Cancer Using Self-Organizing Maps", *Solid State Phenomena*, Vol. Mechatronic Systems and Materials V, Trans Tech Publications Inc., Kreuzstrasse 10, 8635 Durnten-Zurich, Switzerland, ISBN: 978-3-03785-645-1, pp.223-228, (March 2013)
6. A. Świetlicka, K. Gugała, M. Kolasa, J. Pauk, A. Rybarczyk and R.Długosz, "A New Model of the Neuron for Biological Spiking Neural Network Suitable for Parallel Data Processing Realized in Hardware", *Solid State Phenomena*, Vol. Mechatronic Systems and Materials V, Trans Tech Publications Inc., Kreuzstrasse 10, 8635 Durnten-Zurich, Switzerland, ISBN: 978-3-03785-645-1, pp. 217-222, (March 2013)
7. R. Długosz, J. Pauk, P.A. Farine, "New Trends in Motion Capture Systems for Human Gait Analysis", *Machine Graphics and Vision*, A quarterly journal published by: Institute of Computer Science of the Polish Academy of Sciences, (2011)
8. M. Kolasa, R. Długosz, A. Świetlicka, "Wpływ funkcji sąsiedztwa na efektywność uczenia sieci neuronowych Kohonena implementowanych sprzętowo", *Elektryka*, Rok 57., Zeszyt 1 (217), pp. 63–73, (2011)
9. J. Dalecki, T. Talaśka, R. Długosz, "A new, low cost, precise measurement card for testing of ultra-low power analog ASICs", *Elektronika*, No.12, pp. 32–35, (2011)
10. P. Przedwojski, T. Talaśka, R. Długosz, "A Flexible Winner Takes All Neural Network with the conscience mechanism realized on microcontrollers", *Elektronika*, No.12, pp. 14–17, (2011)
11. M. Kolasa, R. Długosz, K. Bieliński, "Programmable, Asynchronous, Triangular Neighborhood Function for Self-Organizing Maps Realized on Transistor Level", *International Journal of Electronics and Telecommunications*, Vol. 56, No. 4, pp. 367–373, (November 2010)
12. R. Długosz, P. Pawłowski, A. Dąbrowski, "Operational amplifier for switched-capacitor systems realized in various CMOS technologies", *Elektronika*, No.1, pp. 67–70, R.51 (2010)
13. S.A. Torbus, M. Kolasa, R. Długosz, "Application of the Kohonen Neural Network in Analysis of the Measurement Results of the Polarization Mode Dispersion", *Bulletin of the University of Technology and Life Sciences, Electronics and Telecommunications series*, Vol. 256, No. 13, pp. 55-66, (December 2010)
14. R. Długosz, T. Talaśka, Przedwojski, "Comparison of Various Hardware Realizations of the Winner Takes All Neural Network", *Bulletin of the University of Technology and Life Sciences, Electronics and Telecommunications series*, Vol. 256, No. 13, pp. 67-78, (December 2010)
15. M. Kolasa R. Długosz, J. Pauk, "A Comparative Study of Different Neighborhood Topologies in WTM Kohonen Self-Organizing Maps", *Journal of Solid State Phenomena*, Trans Tech Publications, Switzerland, Vols. 147–149, pp. 564–569, (2009)
16. J. Pauk, M. Derlatka, R. Długosz, M. Kolasa, "Human Gait Analysis and Classification Based on Neural Networks and Fuzzy Logic", *Journal of Solid State Phenomena*, Trans Tech Publications, Switzerland, Vols. 147–149, pp. 600–605, (2009)
17. R. Długosz, "New Ultra Low Power Switched – Current Finite Impulse Response Filters Realized in CMOS 0.18 μm Technology", *Elektronika*, Vol. 47, No. 10, pp. 26–30, (2006)
18. A. Dąbrowski, R. Długosz, P. Pawłowski, "Rodzina filtrów o skończonej odpowiedzi impulsowej z linią opóźniającą o naprzemiennie połączonych układach opóźniających dwóch typów z przełączanymi kondensatorami" ("Family of the finite impulse response filters with delay line composed of Even and Odd delay elements", *Elektronika*, No. 10/2005, pp.5–8 (2005)
19. A. Dąbrowski, R. Długosz, T. Marciniak, P. Pawłowski, "Projektowanie i realizacja cyfrowych systemów zegarowych do sterowania filtrów FIR-SC", *Elektronika*, No.7, pp. 31–35, (2004)

5.1.3 Chapters in the international monographs

1. M. Kolasa, R. Wojtyna, R. Długosz, W. Jóźwicki, "Application of Artificial Neural Network to Predict Survival Time for Patients with Bladder Cancer", Chapter 11 in *Computers in Medical Activities*, Book series: Advances in Intelligent and Soft Computing, ISSN: 1615-3871, ISBN: 978-3-642-04461-8, Vol. 65 / 2009, pp. 113-122, Springer-Verlag, Berlin / Heidelberg, (2009), **(10 %)**

5.1.4 Participation in various international conferences.

1. P. Skruch, R. Dlugosz, K. Kogut, P. Markiewicz, *et al.*, "The Simulation Strategy and Its Realization in the Development Process of Active Safety and Advanced Driver Assistance Systems", *SAE Technical Paper 2015-01-1401*, Detroit, USA, doi:10.4271/2015-01-1401, (April 2015).
2. M. Kolasa, R. Długosz, W. Pedrycz, "Efficient Initialization of Large Self-Organizning Maps Implemented in the CMOS Technology", *IEEE International Conference on Cybernetics* (CYBCONF), 2015, Gdynia Poland, 24-26 June 2015
3. M. Kolasa, R. Długosz, "An Advanced Software Model for Optimization of Self-Organizing Neural Networks Oriented on Implementation in Hardware", *International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, (June 2015)
4. T. Talaśka, R. Długosz, "Analog Sorting Circuit for the Application in Self-Organizing Neural Networks Based on Neural Gas Learning Algorithm", *International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, (June 2015)
5. R. Długosz, G. Fischer, "Low Chip Area, Low Power Dissipation, Programmable, Current Mode, 10-bits, SAR ADC Implemented in the CMOS 130nm Technology", *International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, (June 2015)
6. R. Długosz, M. Kolasa, T. Talaśka, "A New, Very Efficient Initialization Mechanism for Analog Self-Organizing Neural Networks Implemented in the CMOS Technology", *European Seminar on Computing* (ESCO), Czechy, Pilzno, 15-20.06.2014, str. 71
7. M. Kolasa, T. Talaśka, R. Długosz, "A Novel Recursive Algorithm Used to Model the Hardware Programmable Neighborhood Mechanism of the Self-Organizing Neural Networks", *European Seminar on Computing* (ESCO), Czechy, Pilzno, 15-20.06.2014, str. 70
8. M. Kolasa, R. Długosz, W. Pedrycz, "A fast learning algorithm based on filtering of the quantization error suitable for hardware implemented self-organizing maps", *European Symposium on Artificial Neural Networks, Advances in Computational Intelligence and Learning* (ESANN), Brugia (Belgia), 23-25.04.2014, pp.225-230
9. P. Gurzyński, T. Talaśka, R. Długosz, A. Świetlicka, "An Optimized Algorithm for Recognition of Complex Patterns Based on Artificial Neural Network", *20th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, (June 2013),
10. P. Bethke, R. Długosz, T. Talaśka, "Project and Realization of a Two-Wheels Balancing Vehicle", *20th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, (June 2013),
11. R. Długosz, T. Talaśka, M. Szulc, P. Śniatała, P. Stadelmann, S. Tanner, P.A. Farine, "A low power, low chip area decimation filter for $\Sigma-\Delta$ modulator for flywheel MEMS gyro realized in the CMOS 180 nm technology", *28th International Conference on Microelectronics* (MIEL), Niš, Srbija, pp. 411–414, (13-16 May 2012)
12. R. Długosz, M. Kolasa, M. Szulc, W. Pedrycz, P.A. Farine, "Implementation Issues of Kohonen Self-Organizing Map Realized on FPGA", *15th European Symposium on Artificial Neural Networks* (ESANN), Bruges, Belgium, (April 2012)

13. R. Długosz, T. Talaśka, W. Pedrycz, P.A. Farine, "Analog, Current-Mode Distance Calculation Circuit for Self-Organizing Neural Networks Implemented in CMOS Technology", *15th European Symposium on Artificial Neural Networks* (ESANN), Bruges, Belgium, (April 2012)
14. R. Długosz, T. Talaśka, P.A. Farine, W. Pedrycz, "Convex Combination Initialization Method for Kohonen Neural Network Implemented in the CMOS Technology", *19th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Warszawa, Poland, (May 2012)
15. R. Długosz, M. Kolasa, M. Szulc, "An FPGA Implementation of the Asynchronous Programmable Neighborhood Mechanism for WTM Self-Organizing Map", *18th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gliwice, Poland, (June 2011)
16. T. Talaśka, P. Przedwojski, R. Długosz, "A Flexible Winner Takes All Neural Network with the Conscience Mechanism Realized on Microcontrollers", *18th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gliwice, Poland, (June 2011)
17. J. Dalecki, T. Talaśka, R. Długosz, "A New, Low Cost, Precise Measurement Card for Testing of Ultra-low Power Analog ASICs", *18th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gliwice, Poland, (June 2011)
18. R. Długosz, M. Kolasa, W. Pedrycz, "Fisherman learning algorithm of the SOM realized in the CMOS technology", *14th European Symposium on Artificial Neural Networks* (ESANN), Bruges, Belgium, (April 2011)
19. Rafał Długosz, Tomasz Talaśka, Paweł Przedwojski, Paweł Dmochowski, "A Flexible, Low-Power, Programmable Self-Organizing Neural Network Based on Microcontrollers for Medical Applications", 17$^{\text{th}}$ *Electronics New Zealand Conference* (ENZCon), Hamilton, New Zealand, (November 2010)
20. R. Długosz, M. Kolasa, W. Pedrycz, "Programmable Triangular Neighborhood Functions of Kohonen Self-Organizing Maps Realized in CMOS Technology", *13th European Symposium on Artificial Neural Networks* (ESANN), Bruges, Belgium, April 28–30, pp.529–534, (April 2010)
21. R. Długosz, M. Kolasa, K. Bieliński "Programmable Triangular Neighborhood Function for Kohonen Self-Organizing Map Implemented on Chip", *17th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Wrocław, Poland, pp.328–332, (June 2010)
22. P. Przedwojski, J. Dalecki, T. Talaśka, R. Długosz, "Kohonen Winner Takes All Neural Network Realized on Microcontrollers with AVR and ARM cores", *17th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Wrocław, Poland, pp.273–276, (June 2010)
23. R. Długosz, V. Kolodyazhniy, W. Pedrycz "Power Efficient Hardware Implementation of a Fuzzy Neural Network", *17th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Wrocław, Poland, pp.576–580, (June 2010)
24. R. Długosz, W. Pedrycz, "£ukasiewicz Fuzzy Logic Networks and Their Ultra Low Power Hardware Implementation", *12th European Symposium on Artificial Neural Networks* (ESANN), Bruges, Belgium, pp.275–280, (April 2009)
25. R. Długosz, W. Kolasa, "Optimization of the Neighborhood Mechanism for Hardware Implemented Kohonen Neural Networks", *12th European Symposium on Artificial Neural Networks* (ESANN), Bruges, Belgium, pp.565–570, (April 2009)
26. R. Długosz, M. Kolasa, "A New Fast Training Algorithm for the WTM Kohonen Neural Network Implemented for Classification of Biomedical Signals", *International Conference on Biomedical Electronics and Devices* (BIODEVICES), Porto, Portugal, pp.364–367, (January 2009)

27. R. Długosz, T. Talaśka, "A Low Power Current-Mode Binary-Tree WTA / LTA Circuit for Kohonen Neural Networks", *16th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Łódź, Poland, pp.201–204, (June 2009)
28. R. Długosz, T. Talaśka, R. Wojtyna "Influence of Information Leakage in Analog Memory on Learning Kohonen Network on Silicon", *16th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Łódź, Poland, pp.282–285, (June 2009)
29. R. Długosz, P. Pawłowski, A. Dąbrowski, "Design and Optimization of Operational Amplifiers for SC Systems – a Comparative Study in CMOS 0.8μm, 0.35μm, 0.18μm Technologies", *Signal Processing – Algorithms, Architectures, Arrangements, and Applications* (SPA), Poznań, Poland, pp.36–39, (September 2009)
30. R. Długosz, K. Iniewski, "Power and Area Efficient Circular-Memory Switched-Capacitor FIR Baseband Filter for WCDMA/GSM", *IEEE International Symposium on Circuits and Systems* (ISCAS), Seatle, USA, pp.2326–2329, (May 2008)
31. R. Długosz, V. Gaudet, "Current-mode Memory Cell with Power Down Phase for Discrete Time Analog Iterative Decoders", *IEEE International Symposium on Circuits and Systems* (ISCAS), Seatle, USA, pp.748–751, (May 2008)
32. T. Talaśka, R. Długosz, "Initialization mechanism in Kohonen neural network implemented in CMOS technology", *11th European Symposium on Artificial Neural Networks* (ESANN), Bruges, Belgium, pp.337–342, (April 2008)
33. M. Kolasa, R. Długosz, "Parallel asynchronous neighborhood mechanism for WTM Kohonen network implemented in CMOS technology", *11th European Symposium on Artificial Neural Networks* (ESANN), Bruges, Belgium, pp.331–336, (April 2008)
34. M. Kolasa, R. Długosz, J. Pauk, "Analysis of Various WTM Kohonen Self-Organizing Map Algorithms Used for Data Classification of Biomedical Signals", *4th International Conference, Mechatronic Systems and Materials* (MSM), Bialystok, (July 2008) Poland, pp.187–188
35. J. Pauk, M. Derlatka, R. Długosz, M. Kolasa, "Artificial Intelligence Methods for Data Handling in Gait Analysis", *4th International Conference, Mechatronic Systems and Materials* (MSM), Bialystok, Poland, pp.197, (July 2008)
36. R. Długosz, M. Kolasa, "CMOS, Programmable, Asynchronous Neighborhood Mechanism For WTM Kohonen Neural Network", *15th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Poznan, Poland, pp.197–201, (June 2008)
37. R. Długosz, T. Talaśka, J. Dalecki, R. Wojtyna, "Experimental Kohonen Neural Network Implemented in CMOS 0.18μm Technology", *15th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Poznan, Poland, pp.243–248, (June 2008)
38. T. Talaśka, R. Długosz, J. Dalecki, W. Pedrycz, R. Wojtyna, "CMOS implementation of Conscience Mechanism in Kohonen's Neural Network", *International Conference on Signals and Electronic Systems* (ICSES), Kraków, Poland, pp.101–104, (September 2008)
39. T. Talaska, R. Dlugosz, J. Dalecki, W. Pedrycz, R. Wojtyna, "Experimental results of CMOS-implemented conscience mechanism applied for WTA networks", *International Conference on Signals and Electronic Systems* (ICSES), pp.101–104, (September 2008)
40. R. Długosz, K. Iniewski, "Novel CMOS Analog Signal Processing Technique for Solid-State X-Ray Sensors", *IEEE Northeast Workshop on Circuits and Systems* (NEWCAS), Montreal, Canada, pp.770–771, (August 2007)
41. T. Talaśkaand R. Długosz, "Current Mode Euclidean Distance Calculation Circuit for Kohonen's Neural Network Implemented in CMOS 0.18μm Technology", *Canadian Conference on Electrical and Computer Engineering* (CCECE), Vancouver, Canada, pp.437–440, (April 2007)
42. R. Długosz, V. Gaudet, K. Iniewski, "Asynchronous Clock Generator for Flexible Ultra Low Power Successive Approximation Analog-to-Digital Converters", *Canadian Conference on*

Electrical and Computer Engineering (CCECE), Vancouver, Canada, pp.1649–1652, (April 2007)

43. T. Talaśka, R. Długosz, W. Pedrycz, "Adaptive Weights Change Mechanism for Kohonens's Neural Network Implemented in CMOS 0.18μm Technology", *European Symposium on Artificial Neural Networks* (ESANN), Bruge, Belgium, pp.151–156, (April 2007)
44. R. Długosz, K. Iniewski, "Synchronous and Asynchronous Multiplexer Circuits for Medical Imaging Realized in CMOS 0.18μm Technology", *SPIE International Symposium on Microtechnologies for the New Millennium*, Gran Canaria, Spain, Proc. SPIE, Vol. 6590, pp.65900V; DOI:10.1117/12.721239, (May 2007)
45. R. Długosz, T. Talaśka, "Flexible and Low Power Binary-Tree Current Mode Min/Max Nonlinear Filters Realized in CMOS Technology", *SPIE International Symposium on Microtechnologies for the New Millennium*, Gran Canaria, Spain, May 2007 Proc. SPIE, Vol. 6590, pp.65900L; DOI:10.1117/12.721192, (May 2007)
46. R. Długosz, "Ultra Low Power Switched Current Finite Impulse Response Filter Banks Realized in CMOS 0.18μm technology", *SPIE International Symposium on Microtechnologies for the New Millennium*, Gran Canaria, Spain, May 2007, Proc. SPIE, Vol. 6590, pp.65900H; DOI:10.1117/12.721162, (May 2007)
47. T. Talaśka, R. Długosz, R. Wojtyna, "Current mode Kohonen Naural Network", *International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Ciechocinek, Poland, pp.250–255, (June 2007)
48. R. Długosz, K. Iniewski, "Hierarchical Asynchronous Multiplexer for Readout front-end ASIC for Multi-Element Detectors in Medical Imaging", *International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Ciechocinek, Poland, pp.283–286, (June 2007)
49. T. Talaśka, R. Długosz, R. Wojtyna, "CMOS Implementation of Low Power Kohonen's Neural Network for Medical Applications", *International Conference Computers in Medical Activities* (CiMA), Lódz, Poland, pp.95–96, (September 2007)
50. R. Długosz, K. Iniewski, R. Wojtyna, "Novel CMOS Analog Signal Processing Technique for Solid-State X-Ray Sensors in Medical Imaging Systems", *International Conference Computers in Medical Activities* (CiMA), Lódz Poland, pp.23–25, (September 2007)
51. R. Długosz, R. Wojtyna, "Low Power Fully Parallel Analog 1-D And 2-D Filters for Medical Diagnostics Implemented in CMOS Technology", *Proceeding International Conference Computers in Medical Activities* (CiMA), Lódz Poland, pp.27–28, (September 2007)
52. E. Piwowarska, W. Kuzmicz, G. Farkas, A. Poppe, M. Hristov, E. Manolov, B. Weber, J. Butas, G. Jablonski, A. Jarosz, A. Kos, A. Golda, R. Dlugosz, "AnaDig–An Educational Chip for VLSI Device Characterization" *IEEE International Conference on Microelectronic Systems Education* (MSE), pp.19–20, (2007)
53. R. Długosz, K. Iniewski, T. Talaśka, "0.35μm 22μW Multiphase Programmable Clock Generator for Circular Memory SC FIR Filter for Wireless Sensor Applications", *IEEE Workshop on Signal Processing Systems* (SIPS), Banff, Canada, pp.157–160, (October 2006)
54. T. Talaśka, R. Wojtyna, Długosz, K. Iniewski, W. Pedrycz, "Analog-Counter-Based Conscience Mechanism in Kohonen's Neural Network Implemented in CMOS 0.18 μm Technology", *IEEE Workshop on Signal Processing Systems* (SIPS), Banff, Canada, pp.416–421, (October 2006)
55. K. Boyle, Sai Mohan Kilambi, R. Długosz, K. Iniewski, V. Gaudet, "An Examination of the Effect of Feature Size Scaling on Effective Power Consumption in Analog to Digital Converters", *IEEE Workshop on Signal Processing Systems* (SIPS), Banff, Canada, pp.194–199, (October 2006)
56. R. Długosz, "New Ultra Low Power Switched – Current Finite Impulse Response Filters Realized in CMOS 0.18 μm Technology", *13th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, pp.337–342, (June 2006)

57. R. Długosz, K. Iniewski, "Ultra Low Power Current-mode Algorithmic Analog-to-Digital Converter Implemented in 0.18 μm CMOS Technology for Wireless Sensor Network", *13th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, pp.401–406, (June 2006)
58. T. Talaśka, R. Wojtyna, R. Długosz, K. Iniewski, "Implementation of the Conscience Mechanism for Kohonen's Neural Network in CMOS 0.18 μm Technology", *13th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Gdynia, Poland, pp.310–315, (June 2006)
59. K. Iniewski, V. Axelrad, A. Shibkov,A. Balasinski, S. Magierowski, R. Długosz, A. Dąbrowski "3.125 Gb/s Power Efficient Line Driver with 2-level Pre-emphasis and 2kV HBM ESD Protection", *IEEE International Symposium on Circuits and Systems* (ISCAS), 23–26.05.2005, Kobe, Japan, Vol.2, pp.1154–1157
60. A. Dąbrowski, R. Długosz, P. Pawłowski K. Iniewski, V. Gaudet, "Analog Baseband Filtering Realized Using Switched Capacitor Finite Impulse Response Filter", *VLSI-TSA International Symposium on VLSI Design*, Hsinchu, Taiwan, pp.108–111, (April 2005)
61. R. Długosz, "Search strategy for relevant parasitic elements and reduction of their influence on the operation of SC FIR filters realized in CMOS technology", *SPIE International Symposium on Microtechnologies for the New Millennium 2005*, Sevilla, Spain, Proc. of SPIE Vol. 5837, Bellingham, WA, 2005, pp.1075–1085, (May 2006)
62. R. Długosz R. Wojtyna, "Voltage-buffer-based low-power area-efficient SC FIR filter for wireless communication", *SPIE International Symposium on Microtechnologies for the New Millennium 2005*, Sevilla, Spain, Proc. of SPIE Vol. 5837, Bellingham, WA, 2005, pp.288–299, (May 2006)
63. R. Długosz, P. Pawłowski, A. Dąbrowski, "Multiphase clock generators with controlled clock impulse width for programmable high order SC FIR filter realized in 0.35μm CMOS technology", *SPIE International Symposium on Microtechnologies for the New Millennium 2005*, Sevilla, Spain, Proc. of SPIE Vol. 5837, Bellingham, WA, 2005, pp.1056–1063, (May 2006)
64. R. Długosz, P. Pawłowski, A. Dąbrowski, "Finite Impulse Response Filter Banks Realized in the Switched Capacitor Technique", *17th European Conference on Circuit Theory and Design* (ECCTD), Cork, Ireland, Volume: 3, pp.III/257–III/260, (29.08–01.09.2005)
65. R. Długosz, P. Pawłowski, A. Dąbrowski, "Laboratory of Mixed Analog-Digital Integrated Circuits (Reason - Educhip Project)", *12th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Kraków, Poland, pp.851–856, (June 2005)
66. R. Długosz, P. Pawłowski, A. Dąbrowski, "Family of the Even-Odd Switched Capacitor Finite Impulse Response Filters", *12th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Kraków, Poland, pp.497–500, (June 2005)
67. T. Talaśka, R. Wojtyna, R. Długosz "Hardware Implemented Neural Network Model with Unsupervised Lerning on Silicon", *12th International Conference Mixed Design of Integrated Circuits and Systems* (MIXDES), Kraków, Poland, pp.133–136, (June 2005)
68. R. Długosz, P. Pawłowski, A. Dąbrowski, "Multicriteria Comparison Of Multi-C SC FIR Filter Structures", *IEEE Signal Processing Workshop* (SP), Poznañ, Poland, pp.145–148, (September 2005)
69. R. Długosz, P. Pawłowski, A. Dąbrowski, "Discrete Time Programmable Analog Filter", *International Conference on Electrical Engineering and Circuit Theory* (SPETO), Ustroń, Poland, pp.443–446, (May 2005)
70. R. Długosz, "Metoda Poszukiwania Krytycznych Pojemności Pasożytniczych w Analogowych Filtrach FIR SC Projektowanych w Technologii CMOS", *IV Krajowe Sympozjum Modelowanie i Symulacja Komputerowa w Technice* (MiSKT), Łódź, Poland, pp.63–68, (April 2005)

5.2 Participation in national and international projects

The achievements of the author include the partcipation in the realization of ten specialized integrated circuits (ASIC) implemented in 'full-custom' style in the CMOS 0.8 μm, 0.35 μm, 0.18 μm, and 0.13 μm technologies. The author was the coordinator of seven of these projects starting from the concept to final verification tests. In most cases, the systems were implemented in the collaboration with teams from different universities and industrial institutions in Poland, Canada and Germany. The author participated also in the projects that are not directly related to realization of ASICs. Most of the projects in which he was involved after receiving the doctoral degree was carried out during his staying at Universities and Institutions in Canada, Switzerland and in Germany.

5.2.1 Participation in research projects after obtaining the doctoral degree.

- Participation (as a main contractor) in the project under the framework of the "Pomost" program organized by the Foundation for Polish Science. The project started in February 2014 to end in December of 2015. Project title is: " Development of Novel Ultra Low Power Parallel Artificial Intelligence Circuits for the Application in Wireless Body Area Network Used in Medical Diagnostics ". This is an international project. It includes collaboration with Prof. Witold Pedrycz of the Department of Electrical and Computer Engineering at the University of Alberta in Edmonton, Canada.
- Implementation of selected building blocks of the AFE (*analog front-end electronics*) ASIC for the application in medical imaging in nuclear medicine. The author designed from the ground up the parallel and asynchronous multiplexer for this system, as well as the pulse shaping filter and the peak detector. The multiplexer is described earlier in Section 4.2.5. The project was realized during his staying at the University of Alberta in Edmonton, Canada in the collaboration with Redlen Technologies (`http://www.redlen.com`). The co-operation was coordinated by dr. Krzysztof Iniewski, who supervised the author during his research stay at the University of Alberta in Canada.
- Participation in the implementation of a system consisting of a specialized receiver and transmitter operating with the frequency of 2 GHz. The project was carried out during the internship in the Scanimetrics company from Edmonton (`http://www.scanimetrics.com`). The role of the author was to optimize the system so as to meet the requirements for operation in the respective ranges of temperature, supply voltage and different models of transistors (the so-called 'corner analysis'). The system has been redesigned by the author in such a way that he worked in a much wider range of these parameters than those they were originally expected.
- Implementation of a new, very low-power, successive approximation (SAR) analog-to-digital converter for the application in wireless sensors networks (WSN) and in the AFE ASICs. It was an internal project on the University of Alberta, coordinated by dr. Krzysztof Iniewski. The ADC architecture invented in Canada was recently further developed during the authors's stay in the IHP Microelectronics in Germany (a new 10-bits ADC occupying 0.01 mm^2, realized in the CMOS 0.13 μm technology).
- Participation in the Swiss CTI project entitled: "Flywheel gyroscope: Levitated rotating MEMS for high sensitivity multi-axis gyroscope and multifunctional accelerometer". The project was realized during the stay of the author at EPFL in Switzerland in collaboration with the team of Prof. Christofer Hierold of ETH Zürich (Departement Verfahrenstechnik und Maschinenbau) as well as Colibrys company of Neuchatel (`http://www.colibrys.com`), which specializes in the design and implementation of commercial gyroscopes and accelerometers.

  Description of the project, which concerned the implementation of the gyroscope with six degrees of freedom is located at the following addresses:

http://esplab.epfl.ch/page-9446-en.html and
http://www.aramis.admin.ch/Default.aspx?page=Beteiligte&projectid=25511

In the project the author was responsible for the implementation of the feedback loop that ensures control of the MEMS (*Microelectromechanical systems*) part of the gyro. He designed from the ground up an analog-to-digital converter based on $\Sigma - \Delta$ modulator, PID controller, finite impulse response (FIR) and infinite impulse response (IIR) filters and the Pulse Width Modulation (PWM) block, whose role was to directly provide the MEMS block the control signals. The filters were used for several purposes. One of them was used as a multi-stage decimation filter for the $\Sigma - \Delta$ modulator (see paper 5.1.[11]). The second filter was located out of the control loop, where it has been used to filter out the noise, in order to extract the information about the values of the measured acceleration.

- Implementation of self-organizing Kohonen neural networks as a low-power analog and digital circuits for the application in wireless sensor networks (WSN) used in medical diagnostics. The realized circuits are described in the publications presented in Section 4.2.5. The projects were realized in collaboration with Prof. Witold Pedrycz from the University of Alberta in Canada. This co-operation is still continued.
- 2005 - 2008 Participation in KBN grant 3 T11 C 039 29, entitled "*Multilevel aided design of analog-digital CMOS electronic circuits*".

5.2.2 Participation in research projects prior to obtaining the doctoral degree

- 2002 – 2004 International REASON project (Research and Training Action for System On Chip Design), the EU 5^{th} Framework Programme. The project was coordinated and led by Prof. Wiesław Kuźmicz from the Warsaw University of Technology (Poland). The author in this project was involved in the implementation of the Educhip ASIC.
- 2001 – 2003 "Optimization of Algorithms for Digital Speech Processing and its Enhancement for modern Telecommunication Systems and in Hearing Aids", Polish Government Project No. 7 T11D 005 20.
- 2001 – 2003 "Design and Optimization of Integrated Finite Impulse Response Electronic Filters in the CMOS Technology", Polish Government Project No. 7 T11B 076 21 (PhD project).
- 1999 – 2001 "Design and Hardware CMOS and BiCMOS Realization of Analog Functional Blocks for GSM Receiver", Polish Government Project No. 8 T11B03716
- 1999 – 2000 Implementation of the FIR decimation filter for the analog-to-digital converter based on the $\Sigma - \Delta$ modulator, for the application in the GSM base station. The project was realized during the stay of the author in the IHP Microelectronics in Frankfurt (Oder), Germany.
- 1997 – 1999 Participation in European Union TEMPUS projects: two scientific visits in École Nouvelle d'Ing énieurs en Communication (ENIC), Lille-France and one visit in Centro Studi e Laboratori Telecomunicazioni (CSELT), Turin-Italy (4 months in total)
- 1997 "Development of methods for separation and filtration of digital signals using digital signal processors", Polish Government Project No. 3 P406 007 07

5.3 Awards and scholarships

- 2013 Marshal of the Kuyavian-Pomeranian Voivodeship Award. Category: Science, research and technical progress.
- 2012 Scholarship for experienced researchers granted by DAAD German Foundation (stay in Germany 12/2012 – 02/2013)

- 2012 Invited Professorship scholarship funded by the Institute of Microtechnolgy / EPFL in Switzerland.
- 2010, 2011, 2012 Team Research Awards (1st and 2nd degree) of His Eminence the Rector of UTLS, for outstanding achievements in the field of scientific research.
- 2011 – 2012 Supporting grant (Kolumb Program) – Foundation for Polish Science
- 2006 – 2009 Marie Curie Scholarship (International Outgoing Fellowship), EU 6^{th} Framework Programme. Outgoing phase in the Department of Electrical and Computer Engineering at the University of Alberta in Edmonton, Canada. Return phase at the University of Neuchâtel and in EPFL in Switzerland
- 2005 – 2008 Four grants received from the Canadian Microelectronics Corporation (CMC) for chip implementation.
- 2005 – 2006 Postdoctoral Fellowship granted by Foundation for Polish Science to only 15 young Polish doctors: Location: Department of Electrical and Computer Engineering / University of Alberta, Edmonton, Canada.
- 2005 Award of His Magnificence the Rector of the Poznań University of Technology – for the best PhD thesis in 2004
- 2004 PhD thesis with distinctions at the Faculty of Electrical Engineering of the Poznań University of Technology
- 2002 - 2003 Annual scholarship for young scientists granted by the Foundation for Polish Science, extended then for the following year.
- 1997 - 2010 Twelve awarded papers: International Conferences and Workshops (ESANN, SiPS, MIXDES, SP, ICSES)

5.4 Reviewing articles for scientific journals and conference

- IEEE Transactions on Neural Networks,
- IEEE Transactions on Circuits and Systems,
- IEEE Transactions on Very Large Scale Integration Systems,
- Microelectronics Journal (Elsevier),
- Knowledge Based Systems (Elsevier),
- Applied Soft Computing (Elsevier),
- Applied Mathematics and Computation (Elsevier),
- Circuits, Devices & Systems (IET),
- Circuits, Systems & Signal Processing (Springer),
- VLSI Design Journal (Hindavi),
- Vibroengineering Journal,
- IEEE International Symposium on Circuits and Systems (ISCAS)

5.5 Reviewing scholarship applications

For a period of two years the author served as a reviewer for the scholarship applications under the framework of the "Ventures" program of the Foundation for Polish Science.

5.6 Participation in the organizing committee of the conferences

- 1998 Krajowa Konferencja Teoria Obwodów i Układy Elektroniczne (KKTOiUE)
- 1999-2005 IEEE Signal Processing Workshop

5.7 Teaching

Teaching experience of the author covers a period of over 18 years, i.e. the whole period of his professional career. Teaching activities include conducting regular classes, supervision of both the undergraduate and the graduate students. He also assisted with two Ph.D. theses.

5.7.1 Classes taught currently and in the past

- Electronic circuits (exercises, laboratory)
- Circuit theory (lectures, exercises)
- Analog circuits (exercises, laboratory)
- Programming languages: Java, C/C++ (exercises, laboratory)
- Algorithms and data structures (exercises, laboratory)
- Theory of systems (exercises)
- Artificial intelligence systems (exercises, laboratory)
- Measurement systems (lecture, laboratory)
- Basics of computer engineering (lecture)
- Global networks and multimedia systems (project, laboratory)
- Applications in ICT networks (project)
- Diploma Seminar

The author during his staying in Canada and Switzerland took an active part in the preparation of lectures on Microelectronics. Lectures were conducted in English.

5.7.2 Supervision of students at different levels of education

- Promoter of over fifty bachelor theses, the College of Computer Science and the University of Technology and Life Sciences in Bydgoszcz.
- Active participation in the preparation of the Ph.D. dissertations of Dr. Tomasz Talaśka and Dr. Marta Kolasa, the University of Technology and Life Sciences in Bydgoszcz.
- During his staying at the University of Alberta in Canada he assisted in two Master theses of students supervised by Prof. Krzysztof Iniewski.

A Citations of selected publications including citations not listed in Web of Science database

Most of the citations of the author's papers are available in Web of Science database. However, some of the citations are not listed. They are provided below. Taking these citations into account the Hirsch index equals 5.

a. R. Długosz, K. Iniewski, "Flexible Architecture of Ultra-Low-Power Current-Mode Interleaved Successive Approximation Analog-To-Digital Converter for Wireless Sensor Networks", *VLSI Design Journal*, Hindavi Publishing, VLSI Design, Vol. 2007, Article ID 45269, 2007

The paper was cited 17 times:

1. K. Hansen, C. Reckleben, I. Diehl, M. Bach, P. Kalavakuru, "Pixel-level 8-bit 5-MS/s Wilkinson-type digitizer for the DSSC X-ray imager: Concept study" Elsevier, *Nuclear Instruments and Methods in Physics Research*, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Vol. 629, Issue 1, 11 February 2011, pp.269—276

2. Neena Nambiar, Benjamin J. Blalock, M. Nance Ericson, "A novel current-mode multi-channel integrating ADC", Springer, *Analog Integrated Circuits and Signal Processing*, Vol. 63, Number 2 (2010), pp.283–291, DOI: 10.1007/s10470-009-9393-8
3. Hoi-Jun Yoo, Chris van Hoof, "Introduction to Bio-Medical CMOS IC", Springer, *BIO-MEDICAL CMOS ICS, Integrated Circuits and Systems*, 2011, pp.1–9, DOI: 10.1007/978-1-4419-6597-4_1
4. L. Barboni, M. Valle, "Signal Conditioning System Analysis for Adaptive Signal Processing in Wireless Sensors", Springer, *Sensors and Microsystems, Lecture Notes in Electrical Engineering*, 2010, Vol. 54, Part 4, 291-294, DOI: 10.1007/978-90-481-3606-3_56
5. Binhee Kim, Long Yan, Jerald Yoo, Namjun Cho, and Hoi-Jun Yoo, "An Energy-Efficient Dual Sampling SAR ADC with Reduced Capacitive DAC", *IEEE International Symposium on Circuits and Systems* (ISCAS), 24-27 May 2009, pp.972 – 975
6. Yanjie Xiao, Tantan Zhang, Pui-In Mak, Man-Kay Law, R.P. Martins, "A 0.8 μW 8-bit 1.5–20-pF-input-range capacitance-to-digital converter for lab-on-chip digital microfluidics systems", *IEEE Biomedical Circuits and Systems Conference* (BioCAS), 28-30 November 2012, pp.384 – 387
7. L. Barboni, M. Valle, "Signal-to-noise ratio evaluation for embedded wireless sensor nodes: A novel methodology", *16th IEEE International Conference on Electronics, Circuits, and Systems* (ICECS), 13-16 December 2009, pp. 940 – 943
8. F. Fereydouni_Forouzandeh, O.A. Mohamed, M. Sawan, "Ultra Low Energy Communication Protocol for Implantable Wireless Body Sensor Networks", *6^{t}h International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference* (NEWCAS-TAISA), pp. 57 – 60, 22-25 June 2008,
9. L. Barboni, M. Valle, "Experimental Analysis of Wireless Sensor Nodes Current Consumption", *2nd International Conference on Sensor Technologies and Applications*, (SENSORCOMM), 25-31 August 2008, pp. 401 – 406
10. Salim Al-Ahdab, Reza Lotfi and Wouter A. Serdijn, "A 1-V 225-nW 1kS/s Current Successive Approximation ADC for Pacemakers", *Conference on Ph.D. Research in Microelectronics and Electronics* (PRIME), pp. 1–4, 18-21 July 2010
11. Binhee Kim, Long Yan, Jerald Yoo, and Hoi-Jun Yoo, "A 40fJ/c-s 1 V 10 bit SAR ADC with Dual Sampling Capacitive DAC Topology", *Journal of Semiconductor Technology and Science*, Vol.11, No.1, March, 2011, DOI:10.5573/JSTS.2011.11.1.023, pp.23–32
12. Salim Al-Ahdab, "An Ultra Low Power Fully Integrated Sensor Interface IC for Pacemaker", Thesis: degree of Master of Science, The Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, Nederland
13. Salim Alahdab, R. Lotfi, W. A. Serdijn "A 1-V 416-nW Fully Integrated Sensor Interface IC for Pacemakers", *1 International Workshop on ADC Modelling, Testing and Data Converter Analysis and Design and IEEE 2011 ADC Forum* June 30 - July 1, 2011, Orvieto, Italy, pp. 161–166
14. Neena Balakrishnan Nambiar, "A Current-Mode Multi-Channel Integrating Analog-to-Digital Converter", Doctoral Dissertations, University of Tennessee, Knoxville, Trace: Tennessee Research and Creative Exchange, August 2009
15. E. Maghsoudloo, S. Moradi, A. Arian, "Current mode sensor interface system for biomedical implantable applications", *20th Iranian Conference on Electrical Engineering* (ICEE), 15–17 May 2012, pp.26 – 29
16. Jinxin Song, "Ultra low power Analog-to-Digital Converter for Biomedical Devices", Educational program: Master of Science - System-on-Chip Design, School of Information and Communication Technology, Royal Institute of Technology, March 2011, Stockholm, Sweden

17. L. Barboni, M. Valle, "Battery Current Consumption Measurement System for Lifetime Estimation of Wireless Sensor Nodes", *13th Italian Conference Sensors And Microsystems*, Roma, Italy, 19 – 21 February 2008, pp. 464 – 468

b. R. Długosz, T. Talaśka, W. Pedrycz, R. Wojtyna "Realization of the Conscience Mechanism in CMOS Implementation of Winner-Takes-All Self-Organizing Neural Networks", *IEEE Transactions on Neural Networks*, Vol. 21, Iss.6, pp.961–971, (June 2010)

In addition to 9 citations noted in the Web of Science database, the article was also cited by (**15 citations in total**):

1. H. Hikawa, Y. Maeda, "Improved Learning Performance of Hardware Self-Organizing Map Using a Novel Neighborhood Function", *IEEE Transactions on Neural Networks and Learning Systems*, Vol.PP, Is.99, DOI: 10.1109/TNNLS.2015.2398932, 23 February 2015
2. A. Świetlicka, "Trained stochastic model of biological neural network used in image processing task", Elsevier, *Applied Mathematics and Computation*, Available online 9 January 2015, doi:10.1016/j.amc.2014.12.082
3. D. Shapiro, J. Parri, J.-M Desmarais, *et al.*, "ASIPs for artificial neural networks", *IEEE International Symposium on Applied Computational Intelligence and Informatics* (SACI), 19-21 May 2011, pp.529-533
4. B.P. Bhuvana, "Comparison of Training, Testing and Validation Sets in the Application of Analog Signals", *World Applied Sciences Journal* Vol. 29 Iss. 8, 2014, DOI: 10.5829/idosi.wasj.2014.29.08.1434, , pp.1087-1093
5. B.P. Bhuvana, "Reducing Mismatches in the Analog Signal by Using Levenberg-Marquardt Back Propagation Algorithm", *World Applied Sciences Journal* Vol. 29 Iss. 10, 2014, DOI: 10.5829/idosi.wasj.2014.29.08.1434, , pp.1320-1326
6. P. Derugo, M. Dybkowski, K. Szabat, "Zastosowanie adaptacyjnego neuronowo-rozmytego regulatora prędkości z konkurencyjnymi warstwami Petriego do sterowania silnika elektrycznego", *Przegląd Elektrotechniczny*, 2013, R. 89, nr 12, pp.64-67

c. R. Długosz, T. Talaśka, W. Pedrycz, "Current-Mode Analog Adaptive Mechanism for Ultra-Low Power Neural Networks", *IEEE Transactions on Circuits and Systems–II: Express Briefs*, Vol. 58, Iss. 1, pp. 31–35, (January 2011)

The paper was cited 6 times:

1. K. Roy, D. Fan, X. Fong, *et al*, "Exploring Spin Transfer Torque Devices for Unconventional Computing" *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 5, Iss. 1, March 2015, pp.5-16
2. M. Sharad, C. Augustine, G. Panagopoulos, K. Roy, "Spin based neuron-synapse module for ultra low power programmable computational networks" *International Joint Conference on Neural Networks* (IJCNN), 10-15 June 2012, pp.1-7
3. S. Decherchi, P. Gastaldo, A. Leoncini, R. Zunino, "Efficient Digital Implementation of Extreme Learning Machines for Classification", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 59, Iss. 8, pp.496-500
4. M. Sharad, C. Augustine, G. Panagopoulos, K. Roy, "Spin-Based Neuron Model With Domain-Wall Magnets as Synapse", *IEEE Transactions on Nanotechnology*, Vol.11, Iss.4, pp.843-853
5. A. Świetlicka, "Trained stochastic model of biological neural network used in image processing task", Elsevier, *Applied Mathematics and Computation*, Available online 9 January 2015, doi:10.1016/j.amc.2014.12.082

6. R. Banchuin, "Complete Circuit Level Random Variation Models of Nanoscale MOS Performance", Interational Journal Information and Electronic Engineering, 2011, IJIEE 2011 Vol.1(1): 9-15 ISSN: 2010-3719, DOI: 10.7763/IJIEE.2011.V1.2

d. R. Długosz, W. Pedrycz, "Łukasiewicz Fuzzy Logic Networks and Their Ultra Low Power Hardware Implementation", *Neurocomputing*, Elsevier, doi:10.1016/j.neucom.2009.11.027, Vol. 73, Iss.7-9, pp.1222–1234, (March 2010), **(80 %)**

The paper was cited 5 times:

1. Xingfang Zhang "Duality and pseudo duality of dual disjunctive normal forms *Knowledge-Based Systems*, Vol. 24, Issue 7, October 2011, pp.1033–1036
2. Sun Lihua, Zhang Xingfang, Li Youyu, "Pseudo duality and pseudo law of excluded middle in logic systems", *Computer Engineering and Applications*, 2012, 48 (14), pp.60–62
3. A.H. Zavala, I.Z. Batyrshin, O.C. Nieto, O. Castillo, "Conjunction and disjunction operations for digital fuzzy hardware" *Applied Soft Computing*, 03/2013 13(7), pp.3248-3258.
4. A.H. Zavala, O.C. Nieto, "Fuzzy Hardware: A Retrospective and Analysis" *IEEE Transactions on Fuzzy Systems*, Vol. 20, Iss. 4, pp.623 - 635
5. Article: Genetic algorithms based logic-driven fuzzy neural networks for stability assessment of ru... Mehmet Levent Koç, Can Elmar Balas Applied Ocean Research 08/2012 37:211–219.

e. R. Długosz, T. Talaśka, "Low power current-mode binary-tree asynchronous Min/Max circuit", *Microelectronics Journal*, Elsevier, Vol.41, No.1, pp.64–73, (January 2010)

The paper was cited 5 times

1. T. Mak, Kai-Pui Lam, H. S. Ng, G. Rachmuth, Chi-Sang Poon, "A CMOS Current-Mode Dynamic Programming Circuit", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol.57, Iss.12, July 2010, pp.3112-3123
2. M. Sharad, D. Fan, K. Roy, "Energy-Efficient Non-Boolean Computing With Spin Neurons and Resistive Memory", *IEEE Transactions on Nanotechnology*, Vol.13, Iss.1, January 2014, pp.23-34
3. M. Sharad, D. Fan, K. Roy, "Ultra low power associative computing with spin neurons and resistive crossbar memory", *50th Annual Design Automation Conference* (DAC), Article No. 107, ACM New York, NY, USA, 2013 doi¿10.1145/2463209.2488866
4. M.H. Moaiyeri, R. Chavoshisani, A. Jalali, K. Navi, O. Hashemipour, "High-Performance Mixed-Mode Universal Min-Max Circuits for Nanotechnology", *Circuits, Systems, and Signal Processing*, April 2012, Volume 31, Issue 2, pp.465-488
5. Dai Li, Zhuang Yiqi, Jing Xin, Tang Hualian, "High-Performance CMOS current-mode Winner-take-all circuit", *Journal of Xidian University*, Vol. 39, No. 3, June 2012, pp.80-85

f. R. Długosz, M. Kolasa, W. Pedrycz, M. Szulc, "Parallel Programmable Asynchronous Neighborhood Mechanism for Kohonen SOM Implemented in CMOS Technology", *IEEE Transactions on Neural Networks*, Vol. 22, Iss. 12, pp. 2091–2104, (December 2011)

The paper was cited 5 times:

1. H. Hikawa, Y. Maeda, "Improved Learning Performance of Hardware Self-Organizing Map Using a Novel Neighborhood Function", *IEEE Transactions on Neural Networks and Learning Systems*, Vol.PP, Is.99, DOI: 10.1109/TNNLS.2015.2398932, 23 February 2015

2. A. Świetlicka, "Trained stochastic model of biological neural network used in image processing task", *Applied Mathematics and Computation*, Elsevier, doi:10.1016/j.amc.2014.12.082, 9 January 2015
3. Jicheng Ding, Jian Zhang, Weiquan Huang and Shuai Chen, "Laser Gyro Temperature Compensation Using Modified RBFNN". *Sensors* 14 (10), doi:10.3390/s141018711, pp.18711-18727.
4. F.J. Maldonado, S. Oonk, K. Reichard, J. Pentzer, "SOM with neighborhood step decay for motor current based diagnostics", *IEEE International Conference on Systems, Man and Cybernetics* (SMC), 5-8 Oct. 2014, pp. 2687-2692
5. A. Świetlicka, K. Gugała, A. Jurkowlaniec, P. Śniatała, A. Rybarczyk, *Neural Networks World Journal*, 2015, doi: 10.14311/NNW.2014.24.00?

g. M. Kolasa, R. Długosz, W. Pedrycz, M. Szulc, "Programmable Triangular Neighborhood Function for Kohonen Self-Organizing Map Implemented on Chip", *Neural Networks*, Elsevier, Vol. 25, pp.146–160, (January 2012)

The paper was cited 5 times:

1. H. Hikawa, Y. Maeda, "Improved Learning Performance of Hardware Self-Organizing Map Using a Novel Neighborhood Function", *IEEE Transactions on Neural Networks and Learning Systems*, Vol.PP, Is.99, DOI: 10.1109/TNNLS.2015.2398932, 23 February 2015
2. A. Świetlicka, "Trained stochastic model of biological neural network used in image processing task", *Applied Mathematics and Computation*, Elsevier, doi:10.1016/j.amc.2014.12.082, 9 January 2015
3. Li Penghua, Chai Yi, Cen Ming, Liu Nian, Qiu Yifeng, "A quantum self-organizing mapping neural network" *32nd Chinese Control Conference* (CCC), 26-28 July 2013, pp. 3264 - 3268
4. Li Penghua, Yinguo Li, Dechao Luo, Baomei Qiu "Assessment of Vehicle Emissions using Quantum SOM Neural Network" *Journal of Computational Information Systems*, 10: 4 (2014), pp.1429–1437
5. A. Świetlicka, K. Gugała, A. Jurkowlaniec, P. Śniatała, A. Rybarczyk, *Neural Networks World Journal*, 2015, doi: 10.14311/NNW.2014.24.00?

h. R. Długosz, K. Iniewski, "High-precision analogue peak detector for X-ray imaging applications", *Electronics Letters*, Vol. 43, Issue 8, pp. 440–441, (12 April 2007), **(80 %)**

The paper was cited 4 times (in Web of Science database is one citation from the list below):

1. C. Sawigun, Wannaya Ngamkham, W.A. Serdijn, "An ultra low-power peak-instant detector for a peak picking cochlear implant processor", *IEEE Biomedical Circuits and Systems Conference* (BioCAS), 3-5 Nov. 2010, pp. 222 – 225
2. Ming Zhang, N. Llaser, H. Mathias, "Design and analysis of a switched-capacitor-based peak detector", *IEEE International Symposium on Circuits and Systems* (ISCAS), 15-18 May 2011, pp. 1001 – 1004
3. Lee Tzung-Je Lee, Hsiao Wei-Chih, Wang Chua-Chin, "20 MHz accurate peak detector for FPW allergy biosensor with digital calibration", *13th International Symposium on Integrated Circuits* (ISIC), 12-14 Dec. 2011, pp. 476 – 479
4. G Tidhar, "Gunshot detection system and method", US Patent 8809787 B2, 2014